FIG. 1B

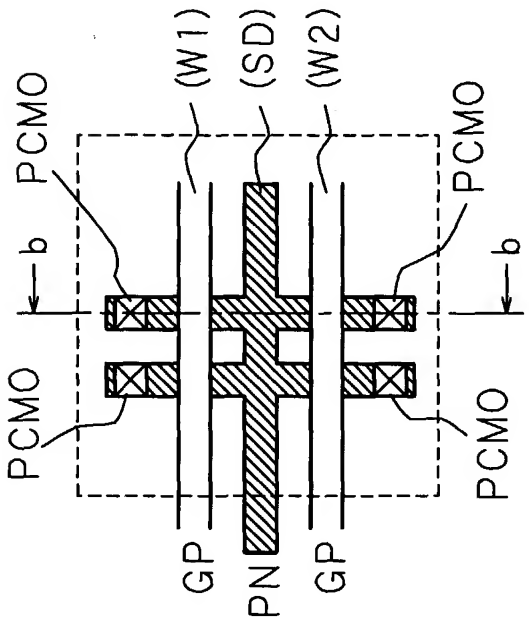


FIG. 1C

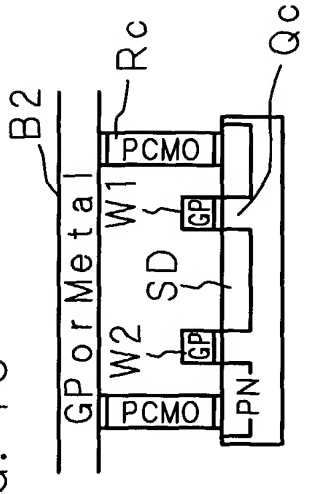
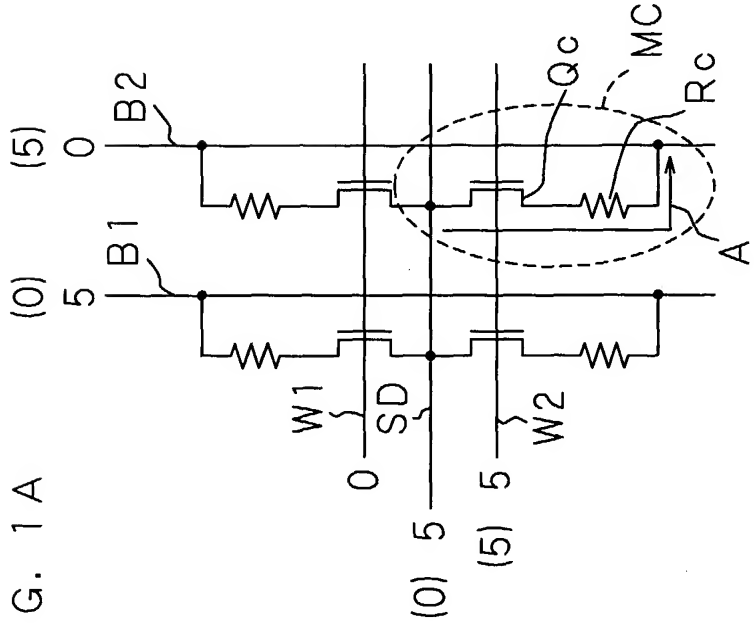


FIG. 1A



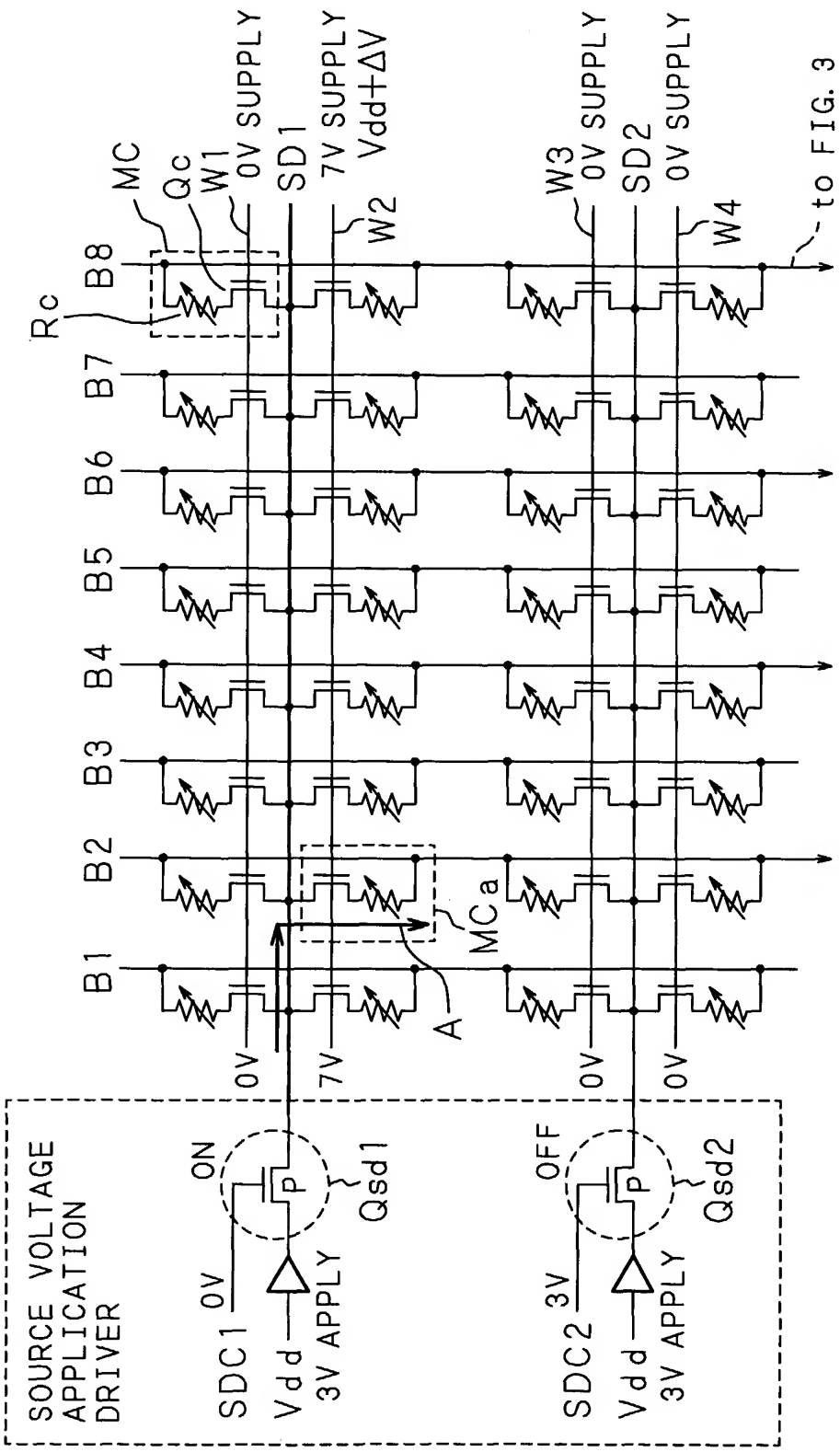

MC
Qc
W1
0V SUPPLY
SD1
7V SUPPLY
Vdd+ΔV
W2
W3
0V SUPPLY
SD2
0V SUPPLY
W4
to FIG. 3
Rc
B8
B7
B6
B5
B4
B3
B2
B1
MCa
A
0V
7V
0V
0V
SOURCE VOLTAGE APPLICATION DRIVER
ON
P
Qsd1
SDC1
0V
Vdd
3V APPLY
OFF
P
Qsd2
SDC2
3V
Vdd
3V APPLY

FIG. 2

FIG. 3

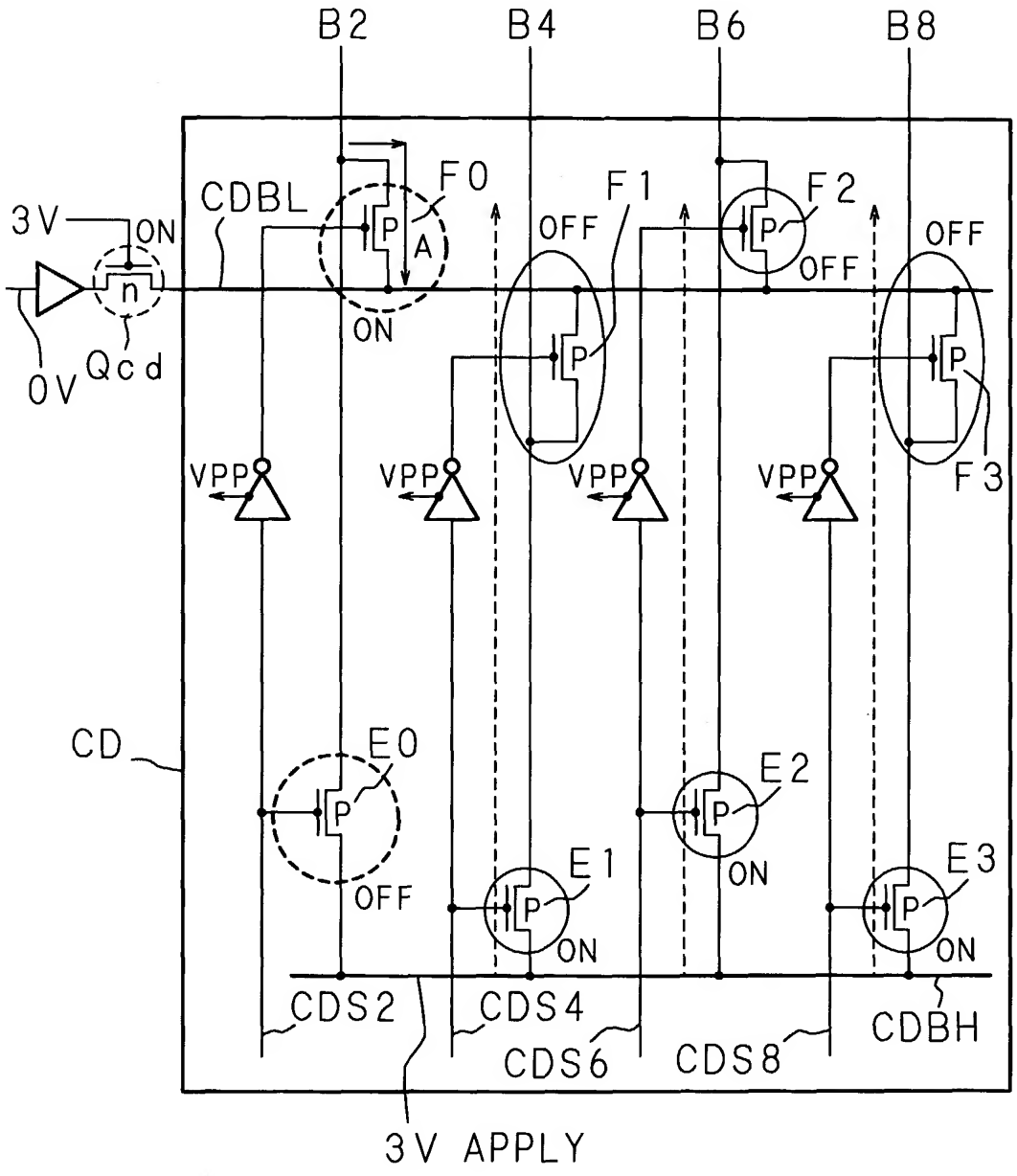

B2
B4
B6
B8
3V
ON
CDBL
F0
P
A
F1
OFF
F2
OFF
OFF
n
ON
0V
Qcd
P
P
P
VPP
VPP
VPP
VPP
F3
CD
E0
P
OFF
E2
P
ON
E1
P
ON
E3
P
ON
CDS2
CDS4
CDS6
CDS8
CDBH
3V APPLY

FIG. 4

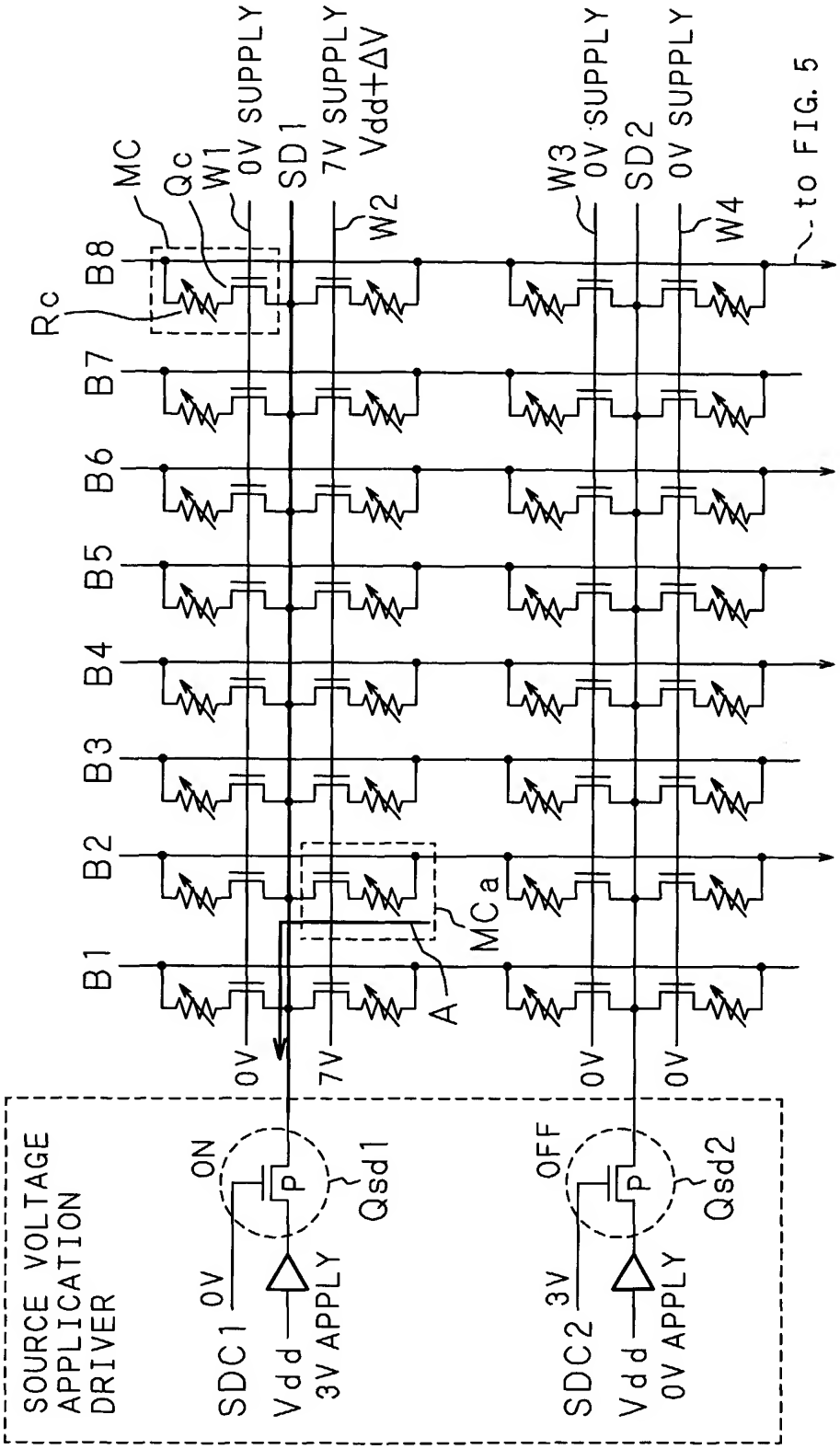
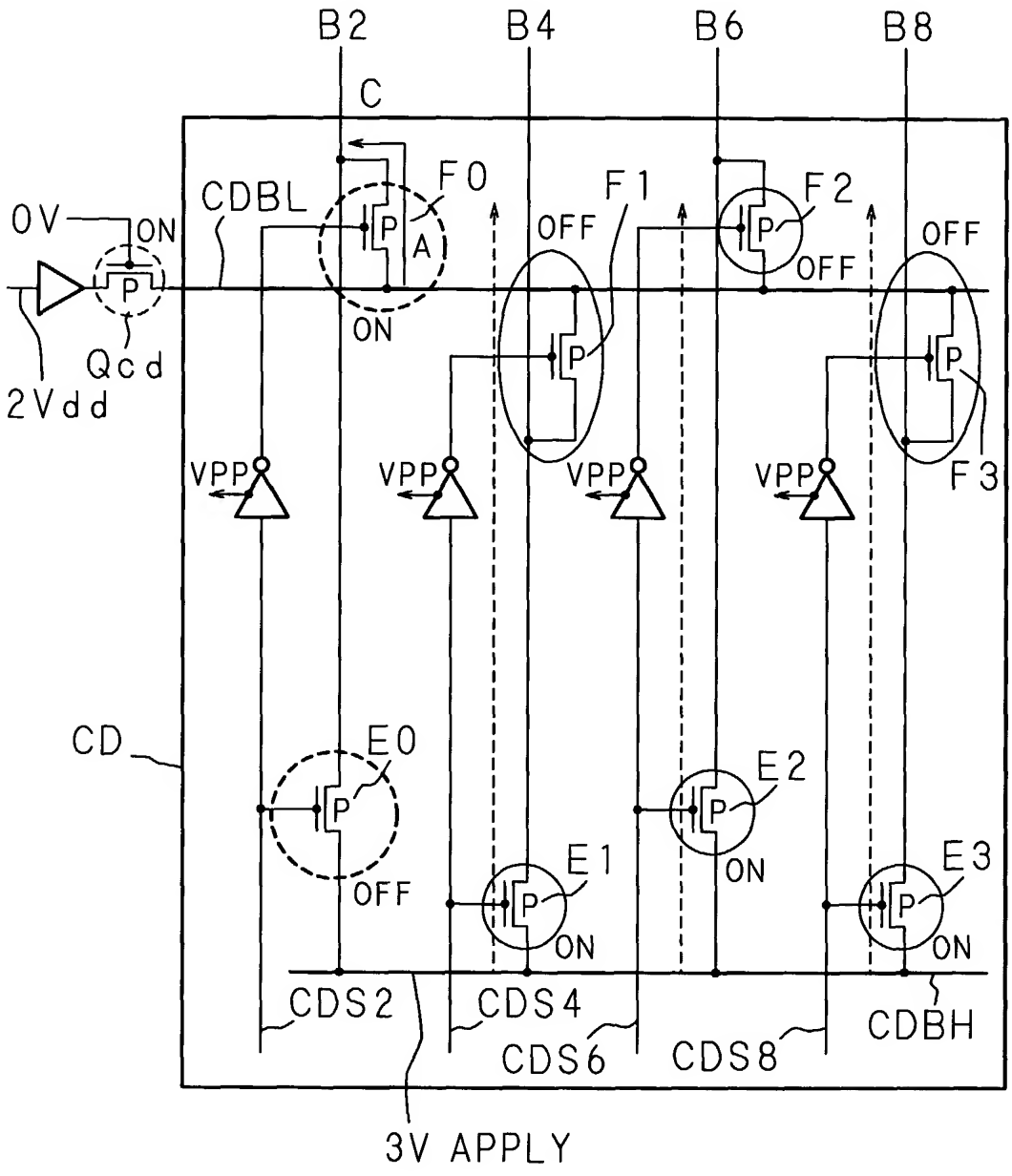

SOURCE VOLTAGE APPLICATION DRIVER
SDC1
0V
Vdd
3V APPLY
ON
P
Qsd1
SDC2
3V
Vdd
0V APPLY
OFF
P
Qsd2
0V
7V
0V
0V
A
MCa
B1
B2
B3
B4
B5
B6
B7
B8
Rc
MC
Qc
W1
0V SUPPLY
SD1
7V SUPPLY
Vdd+ΔV
W2
W3
0V SUPPLY
SD2
0V SUPPLY
W4
to FIG. 5

FIG. 5


B2
B4
B6
B8
C
0V
ON
CDBL
F0
P
A
F1
OFF
F2
OFF
OFF
ON
Qcd
2Vdd
VPP
VPP
VPP
VPP
F3
CD
E0
P
OFF
E1
ON
E2
ON
E3
ON
CDS2
CDS4
CDS6
CDS8
CDBH
3V APPLY

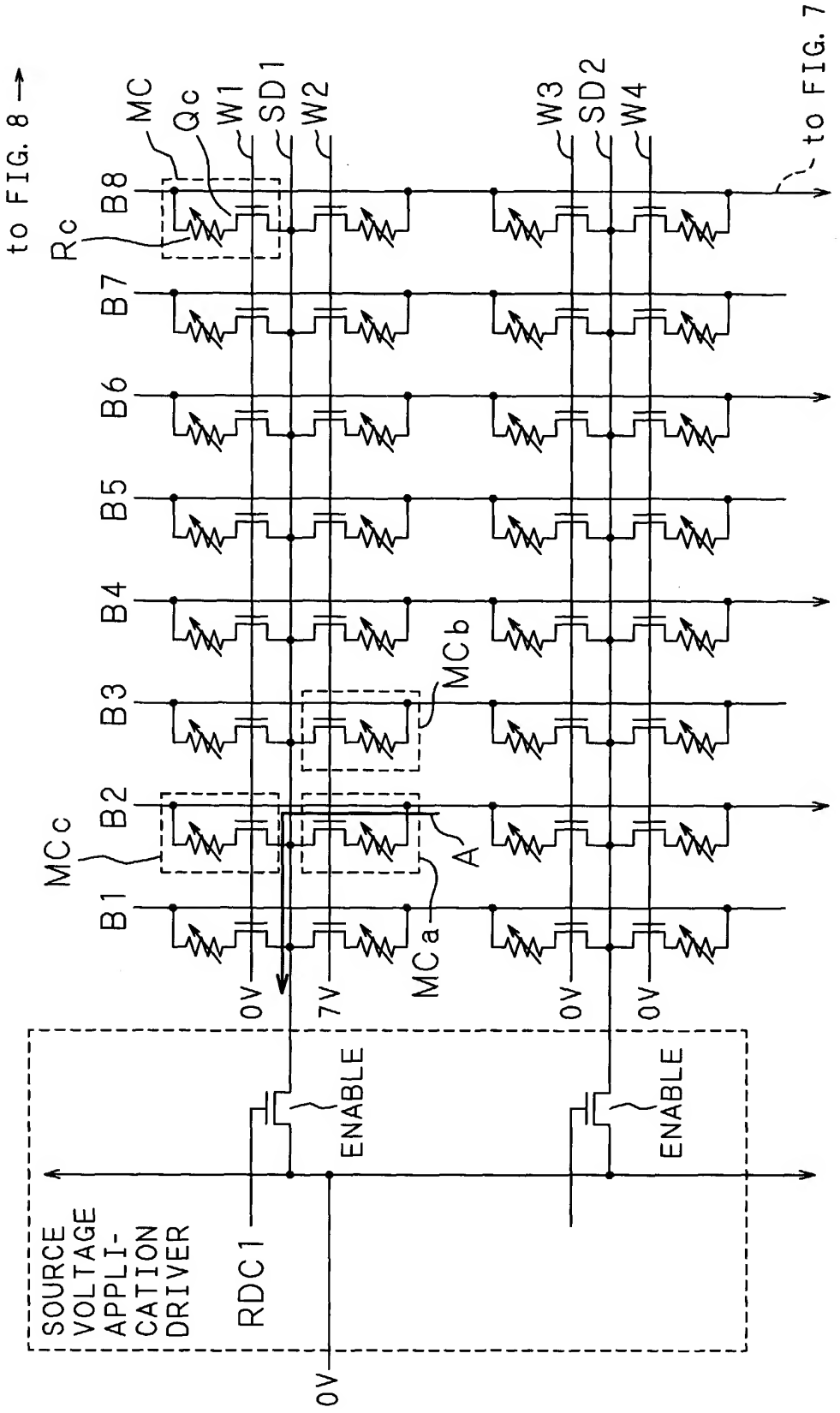

to FIG. 8
to FIG. 7
MC
Qc
W1
SD1
W2
W3
SD2
W4
Rc
B8
B7
B6
B5
B4
B3
B2
B1
MCb
MCc
MCa
A
0V
7V
0V
0V
ENABLE
ENABLE
SOURCE VOLTAGE APPLI-CATION DRIVER
RDC1
0V

FIG. 6

FIG. 7

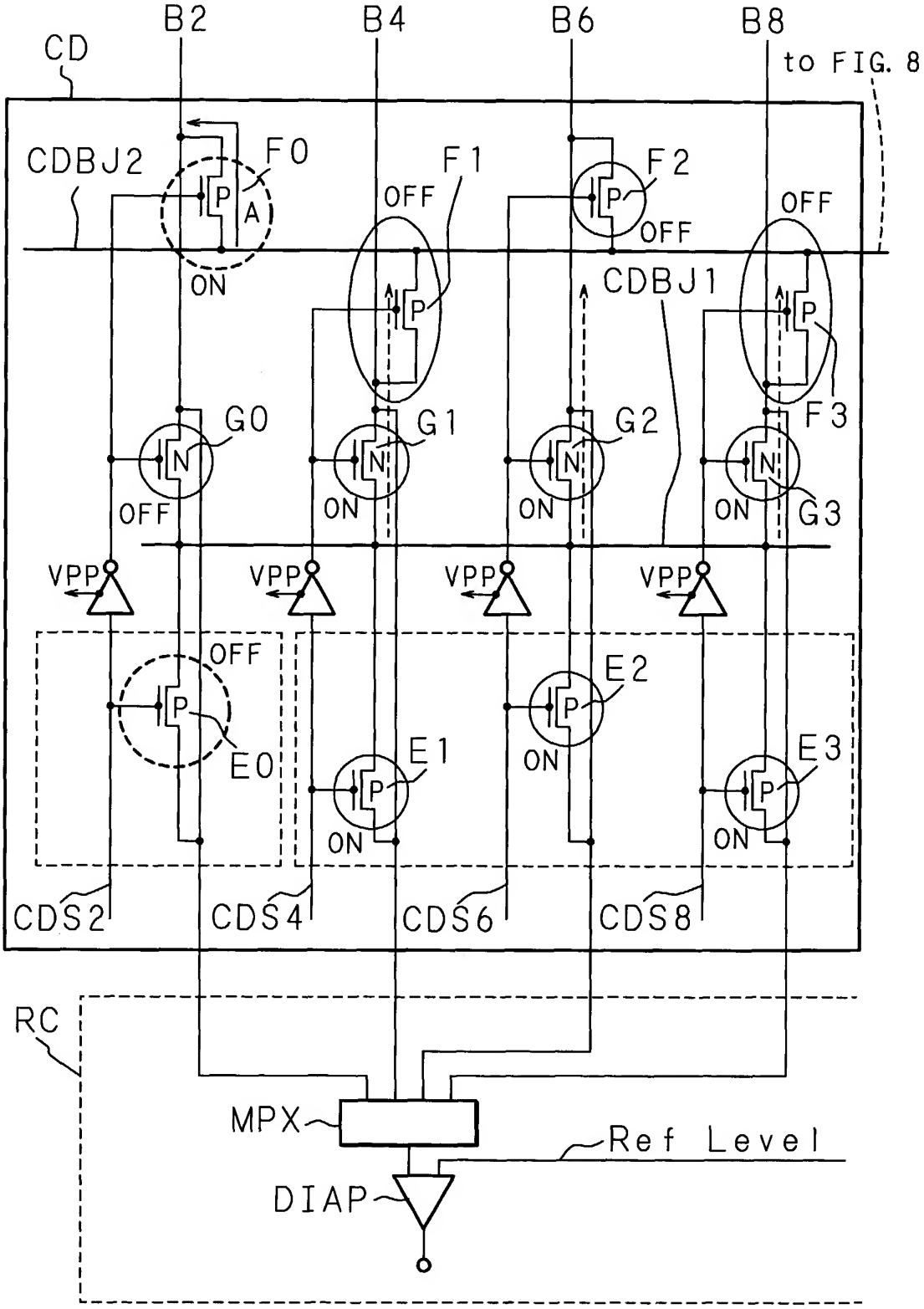

B2
B4
B6
B8
CD
to FIG. 8
CDBJ2
F0
F1
F2
OFF
OFF
OFF
ON
CDBJ1
P
A
G0
G1
G2
F3
N
OFF
ON
ON
ON
G3
VPP
VPP
VPP
VPP
OFF
E2
E0
E1
E3
ON
ON
ON
CDS2
CDS4
CDS6
CDS8
RC
MPX
Ref Level
DIAP

FIG. 8

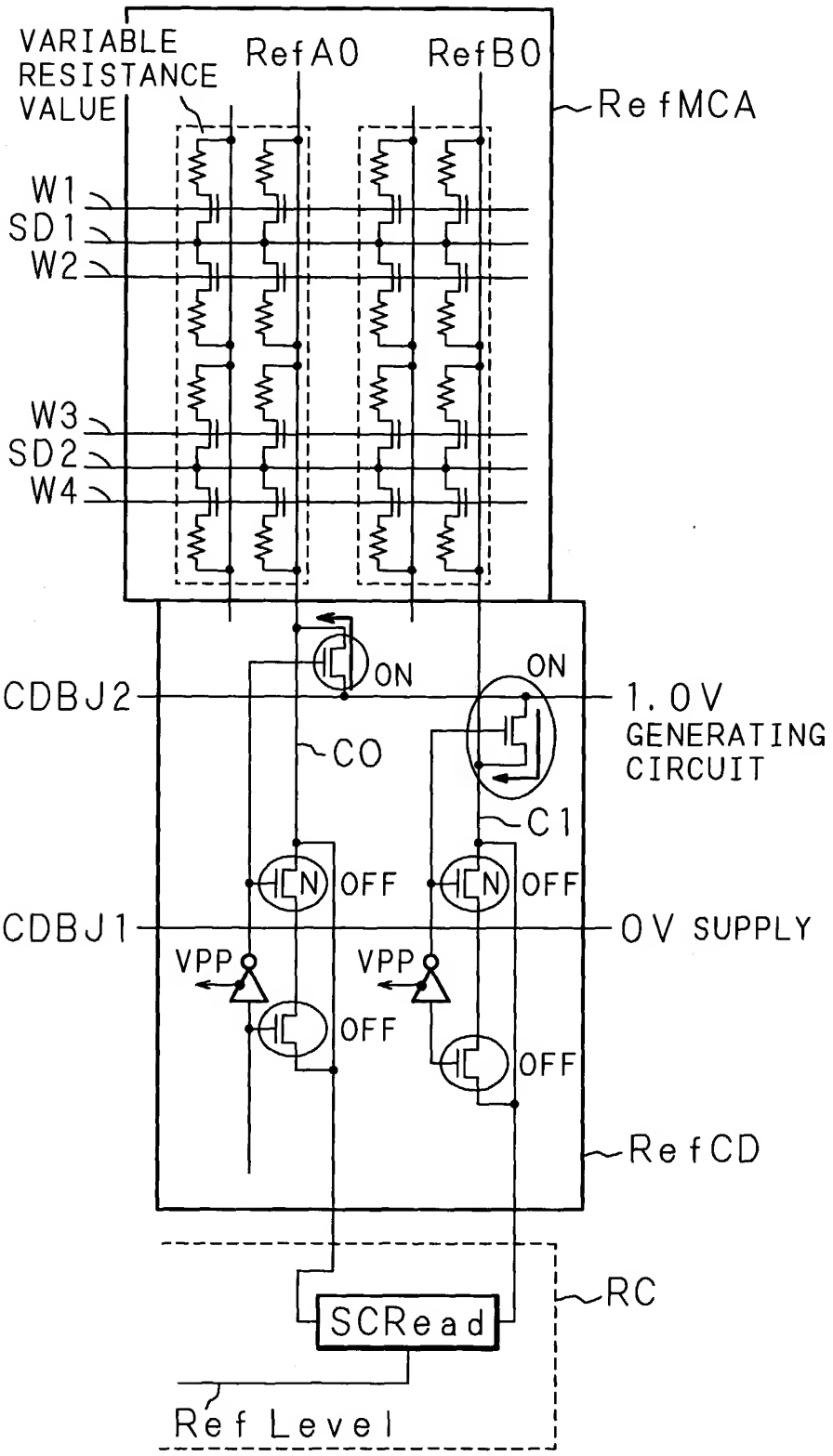

VARIABLE RESISTANCE VALUE
RefA0
RefB0
RefMCA
W1
SD1
W2
W3
SD2
W4
ON
ON
CDBJ2
1.0V GENERATING CIRCUIT
CO
C1
OFF
OFF
CDBJ1
0V SUPPLY
VPP
VPP
OFF
OFF
RefCD
RC
SCRead
Ref Level

FIG. 9

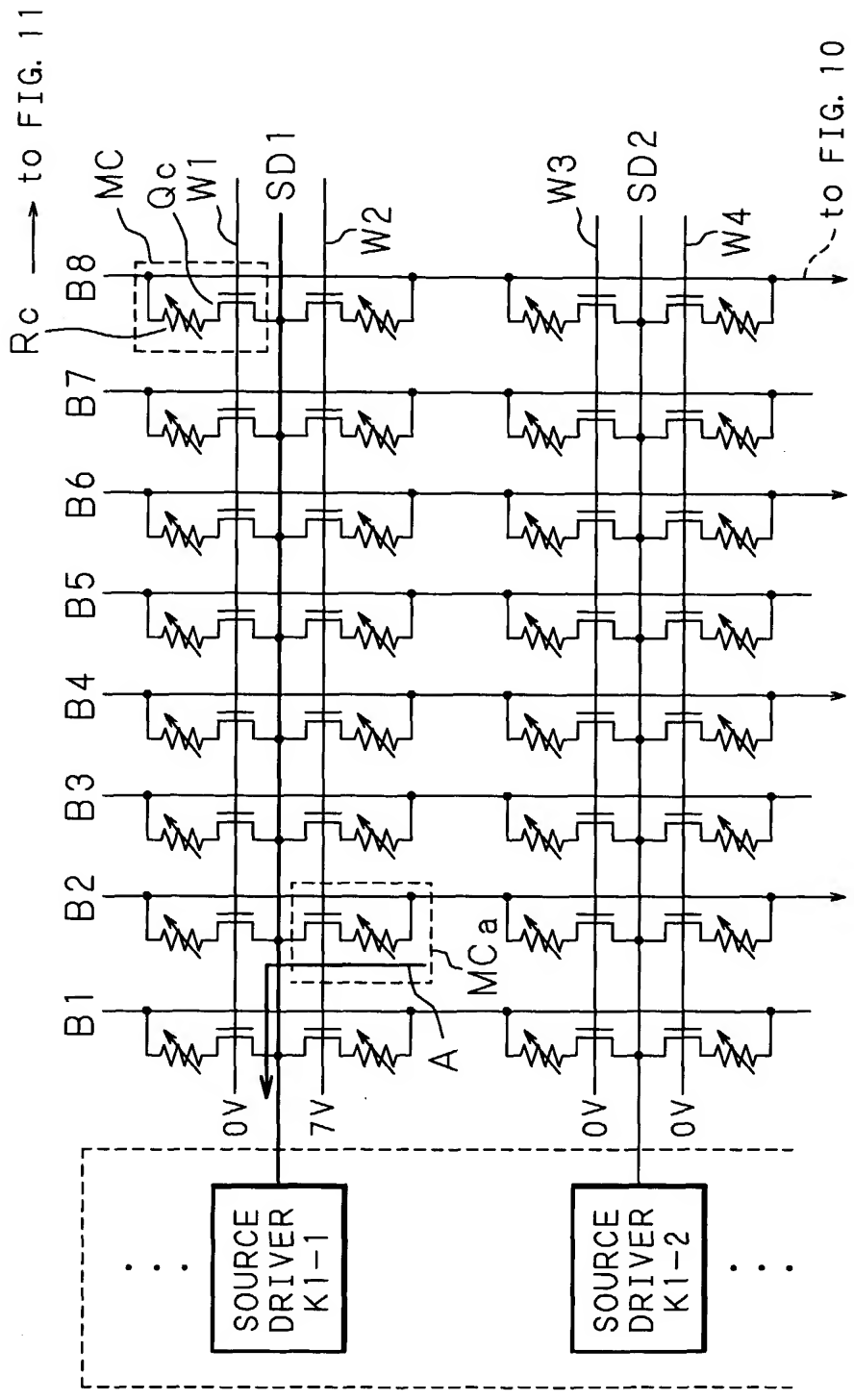

Rc
to FIG. 11
to FIG. 10
MC
Qc
W1
SD1
W2
W3
SD2
W4
B8
B7
B6
B5
B4
B3
B2
B1
MCa
A
0V
7V
0V
0V
SOURCE DRIVER K1-1
SOURCE DRIVER K1-2

FIG. 10

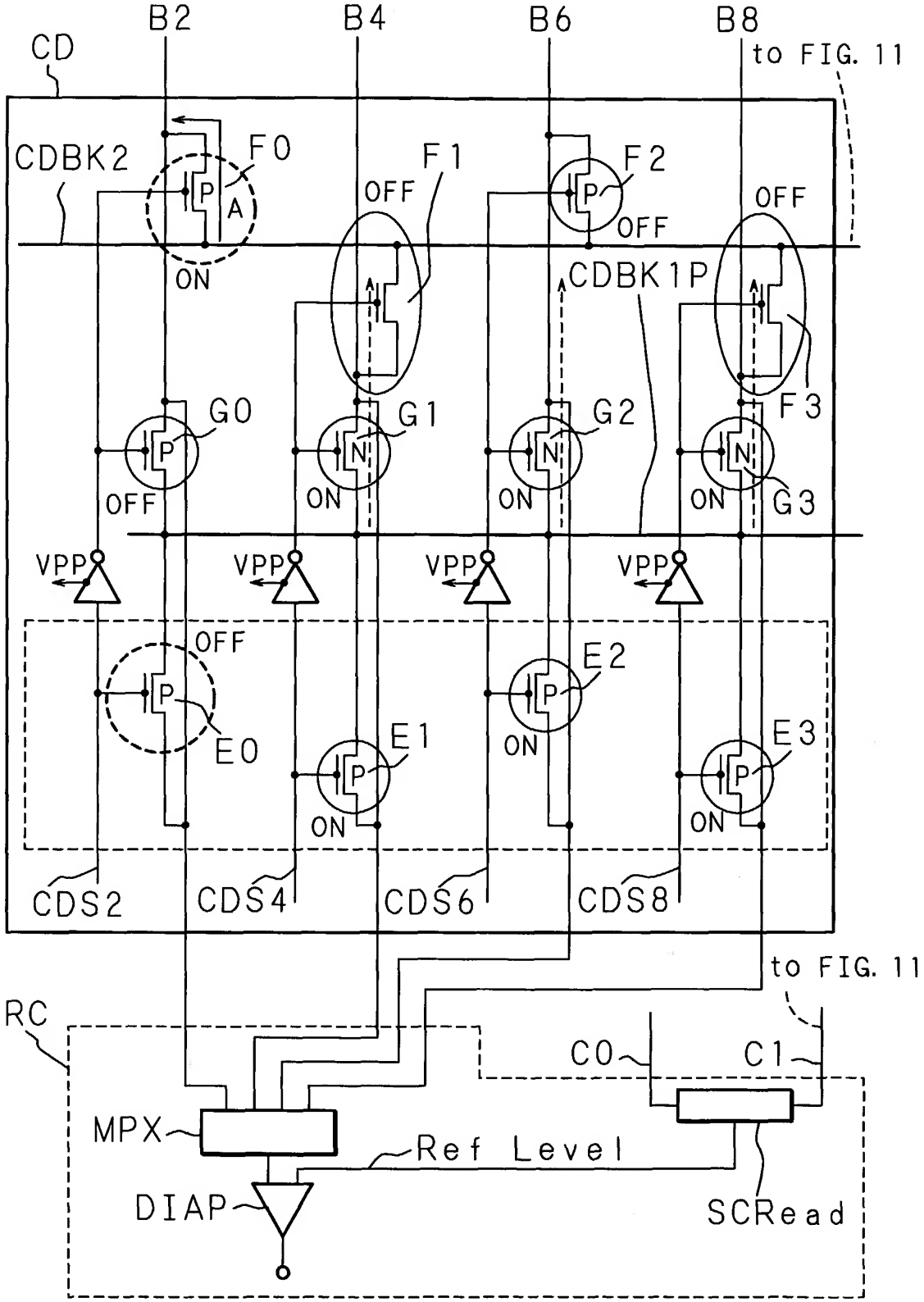

B2
B4
B6
B8
CD
to FIG. 11
CDBK2
F0
P
A
ON
F1
OFF
F2
P
OFF
OFF
CDBK1P
G0
P
OFF
G1
N
ON
G2
N
ON
F3
N
ON
G3
VPP
VPP
VPP
VPP
OFF
P
E0
E1
P
ON
E2
P
ON
E3
P
ON
CDS2
CDS4
CDS6
CDS8
to FIG. 11
RC
C0
C1
MPX
Ref Level
DIAP
SCRead

FIG. 11

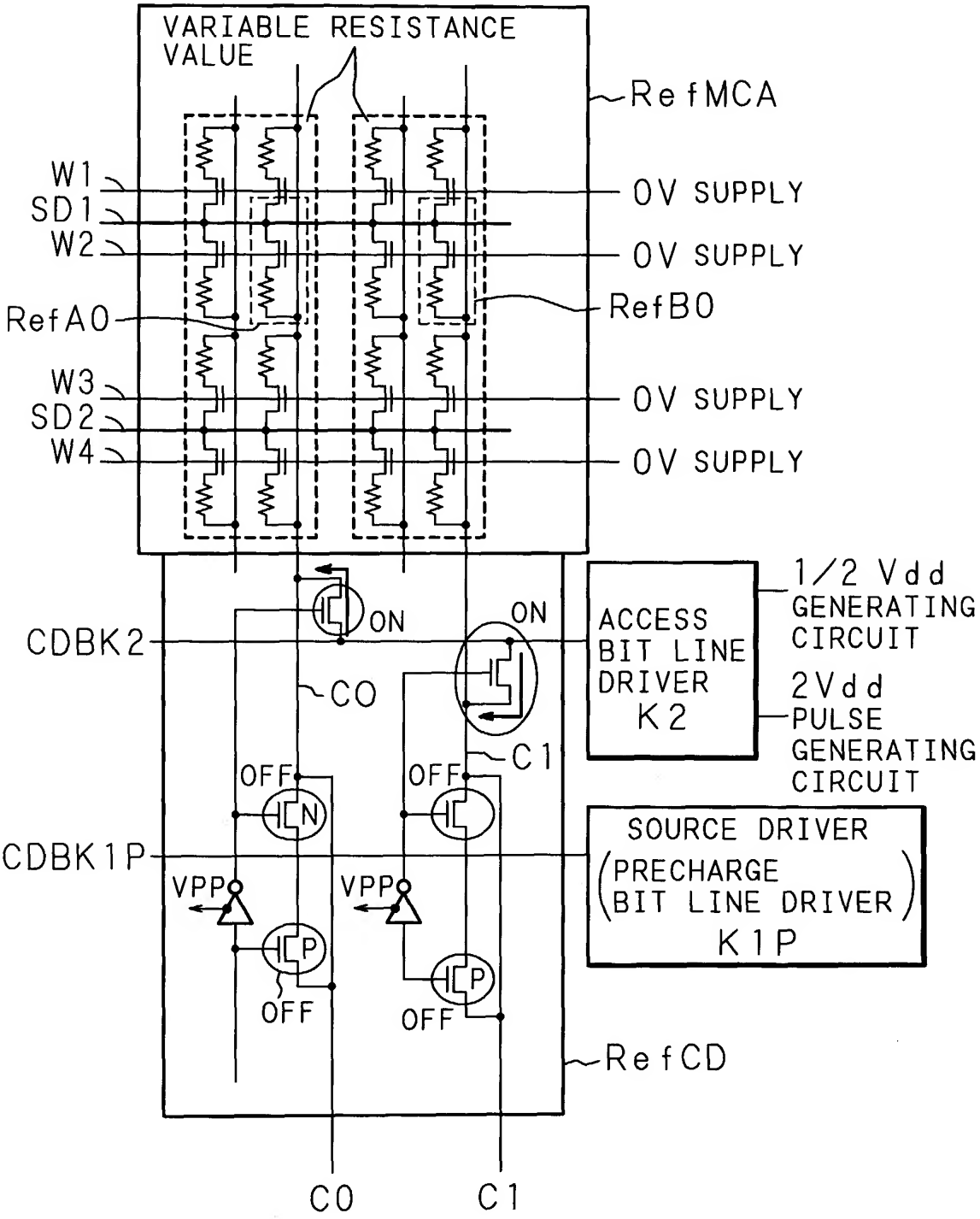

VARIABLE RESISTANCE VALUE
RefMCA
W1
SD1
W2
RefA0
W3
SD2
W4
0V SUPPLY
0V SUPPLY
RefB0
0V SUPPLY
0V SUPPLY
CDBK2
ON
ON
CO
C1
ACCESS BIT LINE DRIVER K2
1/2 Vdd GENERATING CIRCUIT
2Vdd PULSE GENERATING CIRCUIT
OFF
OFF
CDBK1P
SOURCE DRIVER (PRECHARGE BIT LINE DRIVER) K1P
VPP
VPP
OFF
OFF
RefCD
C0
C1

FIG. 12A

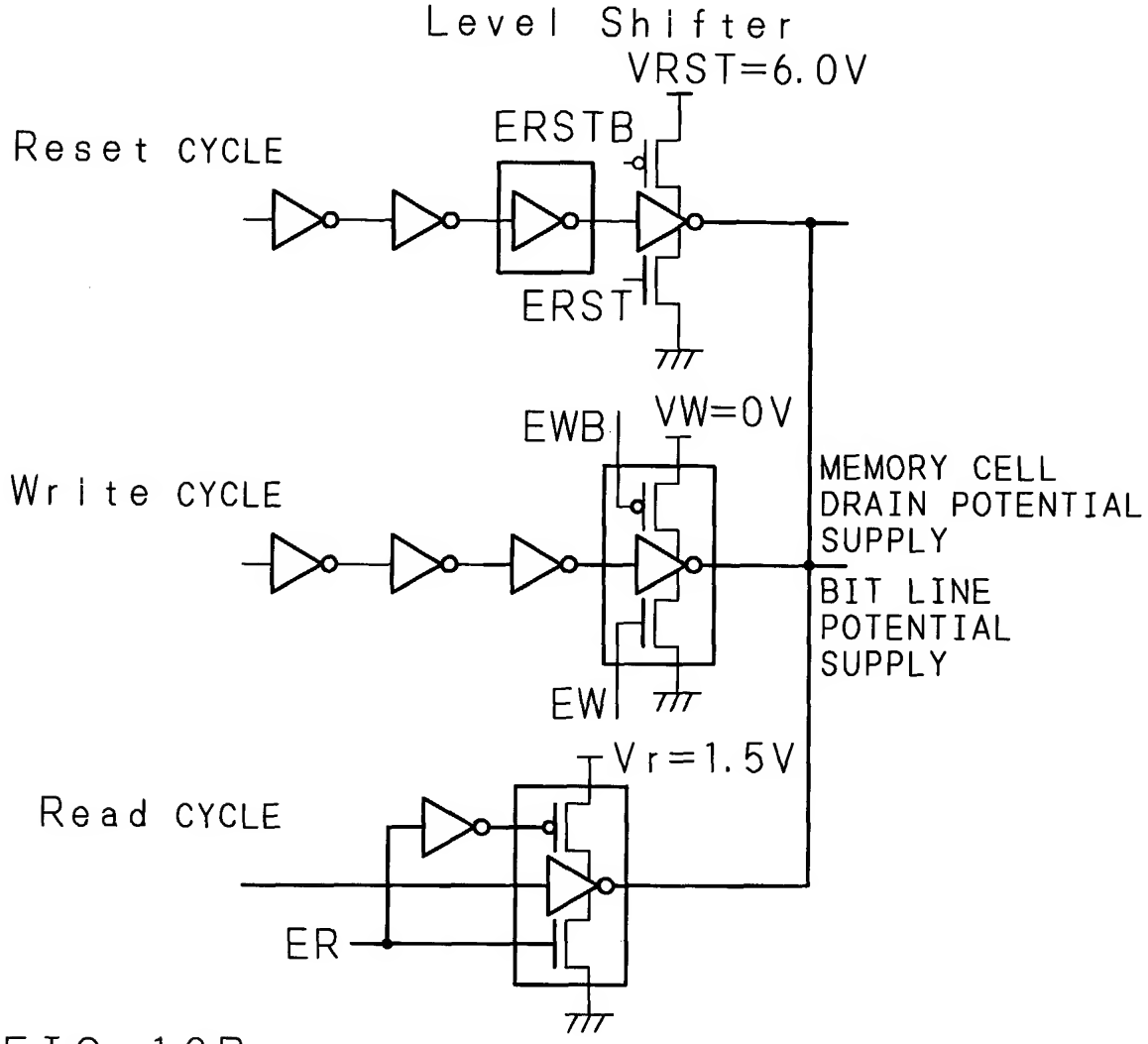


FIG. 12B

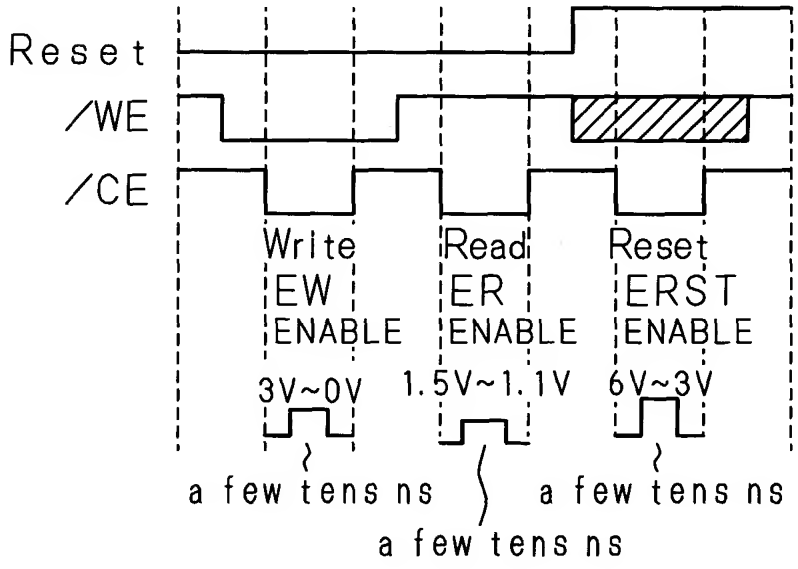


FIG. 13

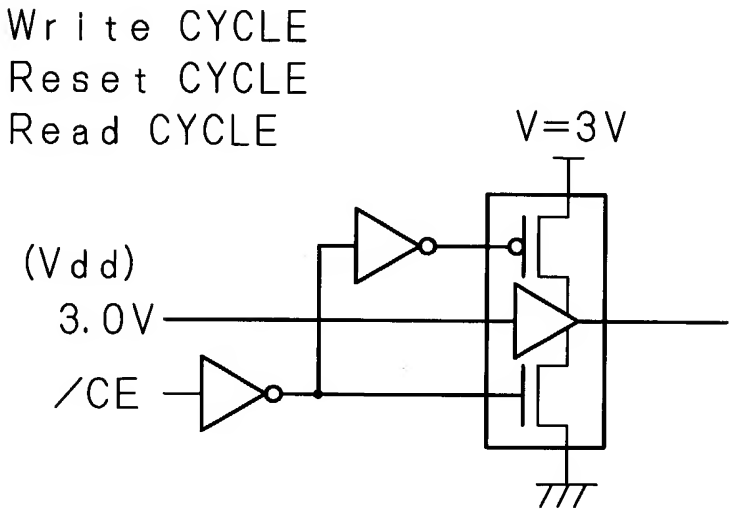
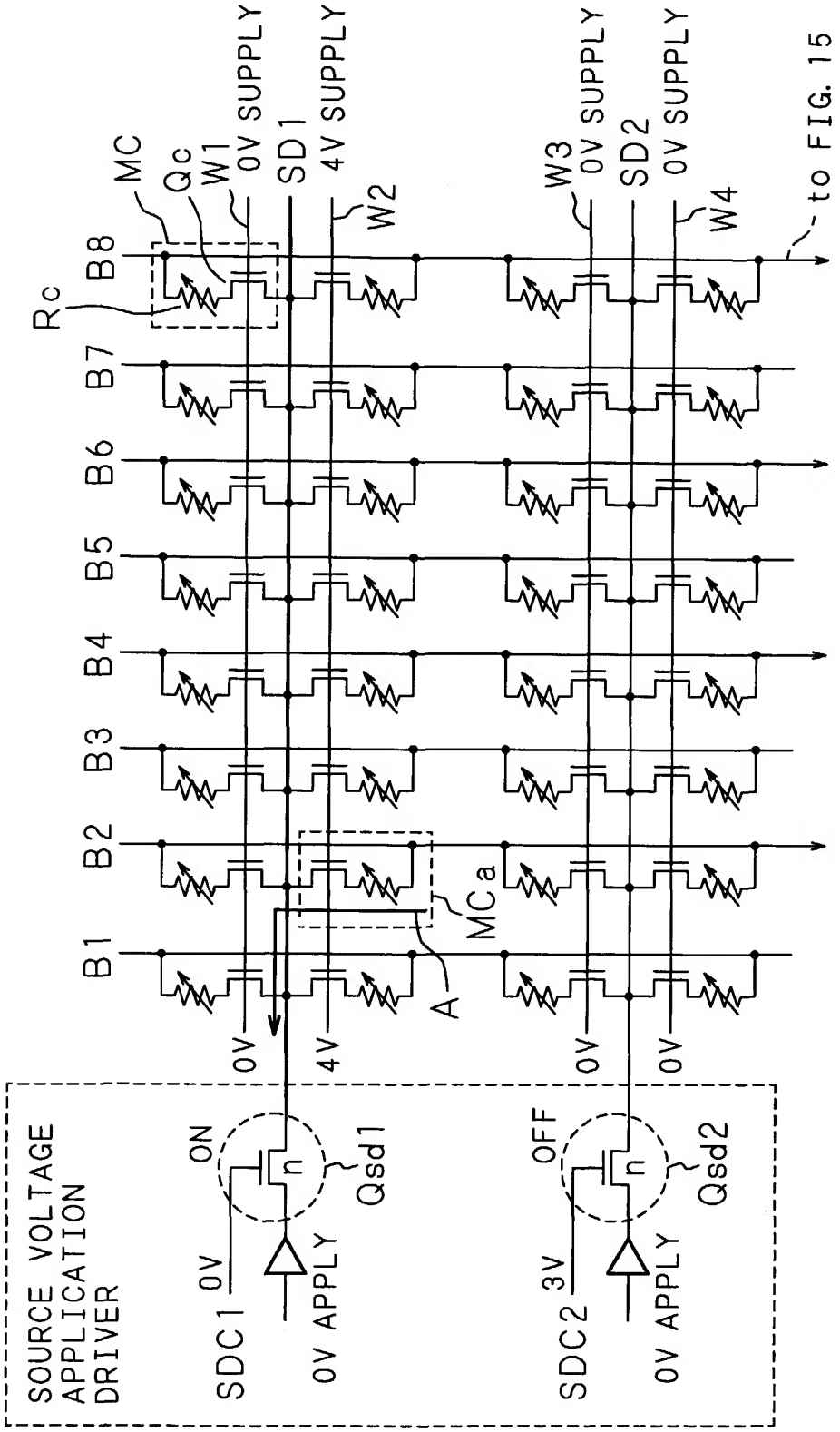


FIG. 14


SOURCE VOLTAGE APPLICATION DRIVER
SDC1
0V
ON
n
Qsd1
0V APPLY
SDC2
3V
OFF
n
Qsd2
0V APPLY
0V
4V
0V
0V
A
MCa
B1
B2
B3
B4
B5
B6
B7
B8
Rc
MC
Qc
W1
0V SUPPLY
SD1
4V SUPPLY
W2
W3
0V SUPPLY
SD2
0V SUPPLY
W4
to FIG. 15

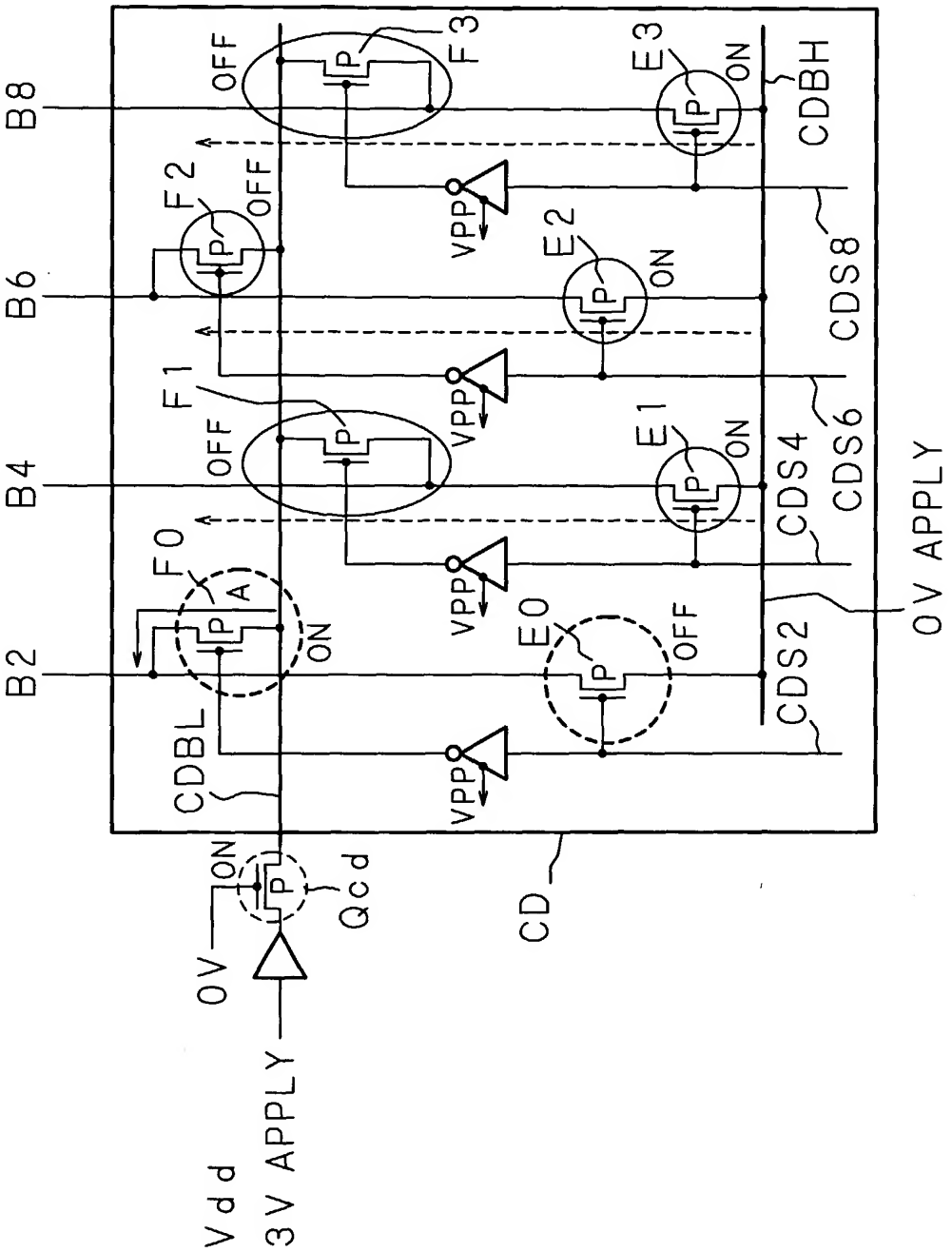

B8
B6
B4
B2
F3
F2
F1
F0
E3
E2
E1
E0
OFF
ON
VPP
CDBH
CDS8
CDS6
CDS4
CDS2
0V APPLY
CDBL
CD
Qcd
0V
3V APPLY
Vdd

FIG. 15

FIG. 16

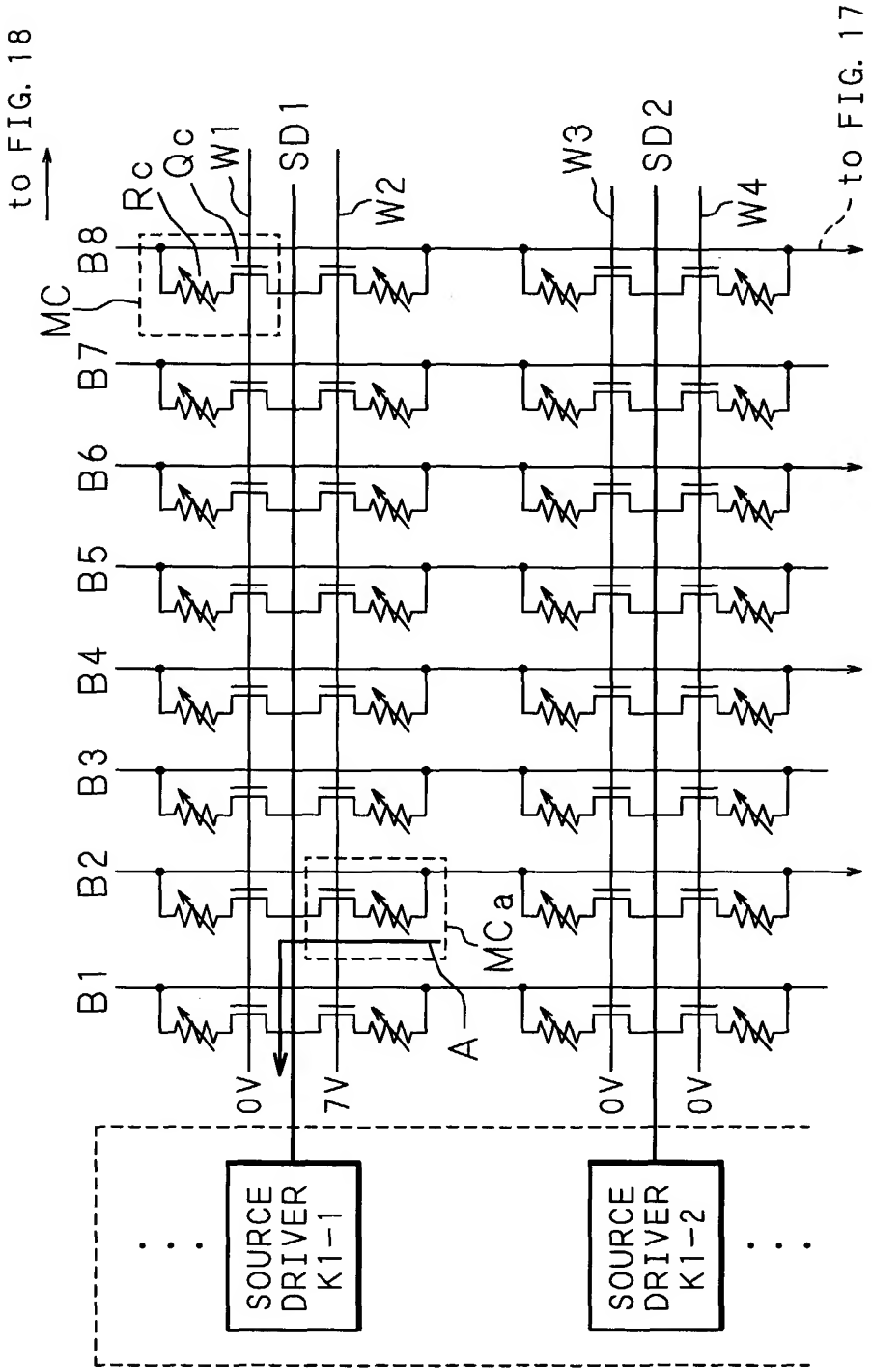

to FIG. 18
to FIG. 17
MC
B8
B7
B6
B5
B4
B3
B2
B1
Rc
Qc
W1
SD1
W2
W3
SD2
W4
MCa
A
0V
7V
0V
0V
SOURCE DRIVER K1-1
SOURCE DRIVER K1-2

FIG. 17

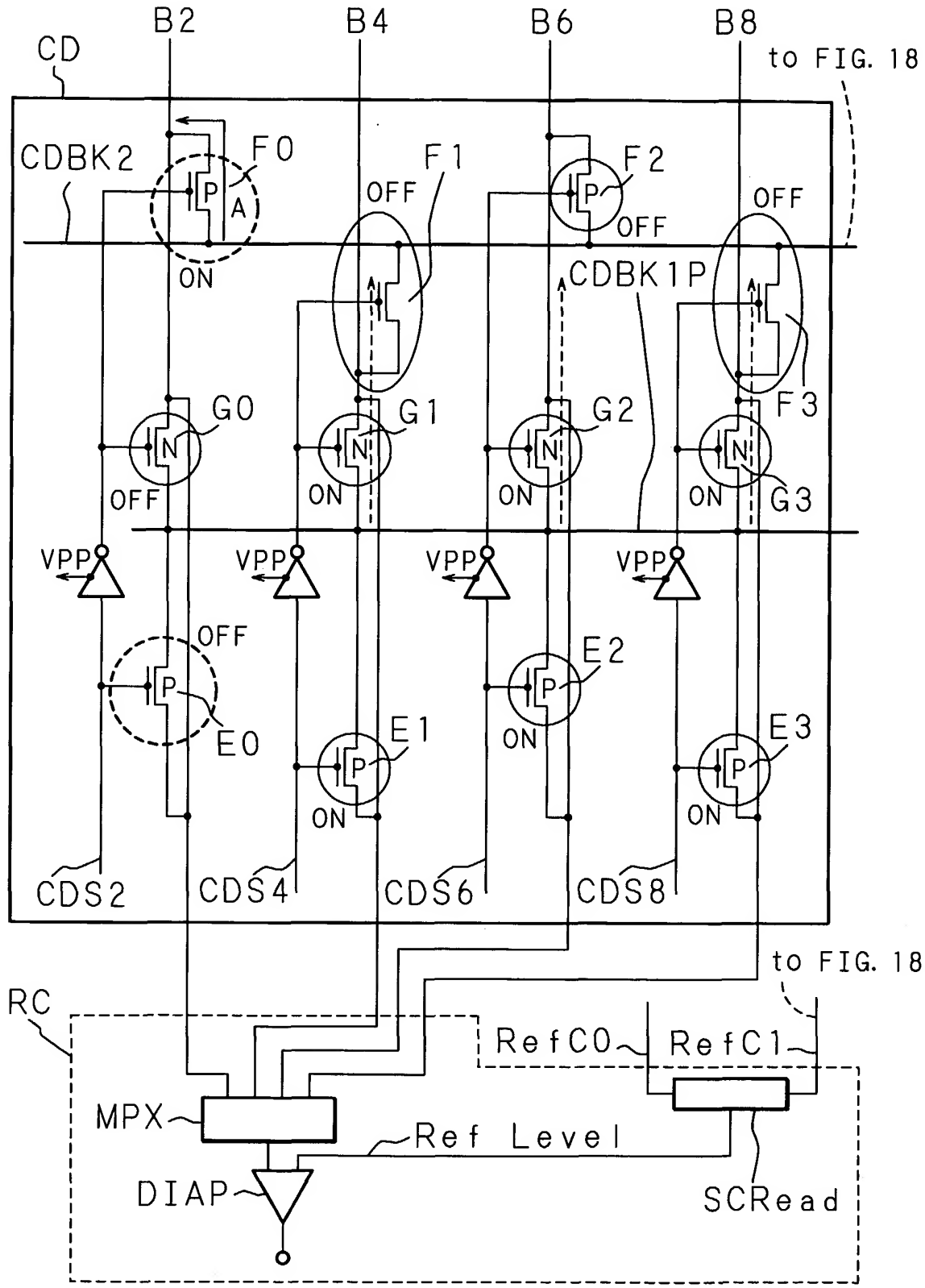

B2
B4
B6
B8
CD
to FIG. 18
CDBK2
F0
F1
F2
F3
P
A
OFF
ON
CDBK1P
G0
G1
G2
G3
N
VPP
E0
E1
E2
E3
CDS2
CDS4
CDS6
CDS8
to FIG. 18
RC
RefC0
RefC1
MPX
Ref Level
DIAP
SCRead

FIG. 18

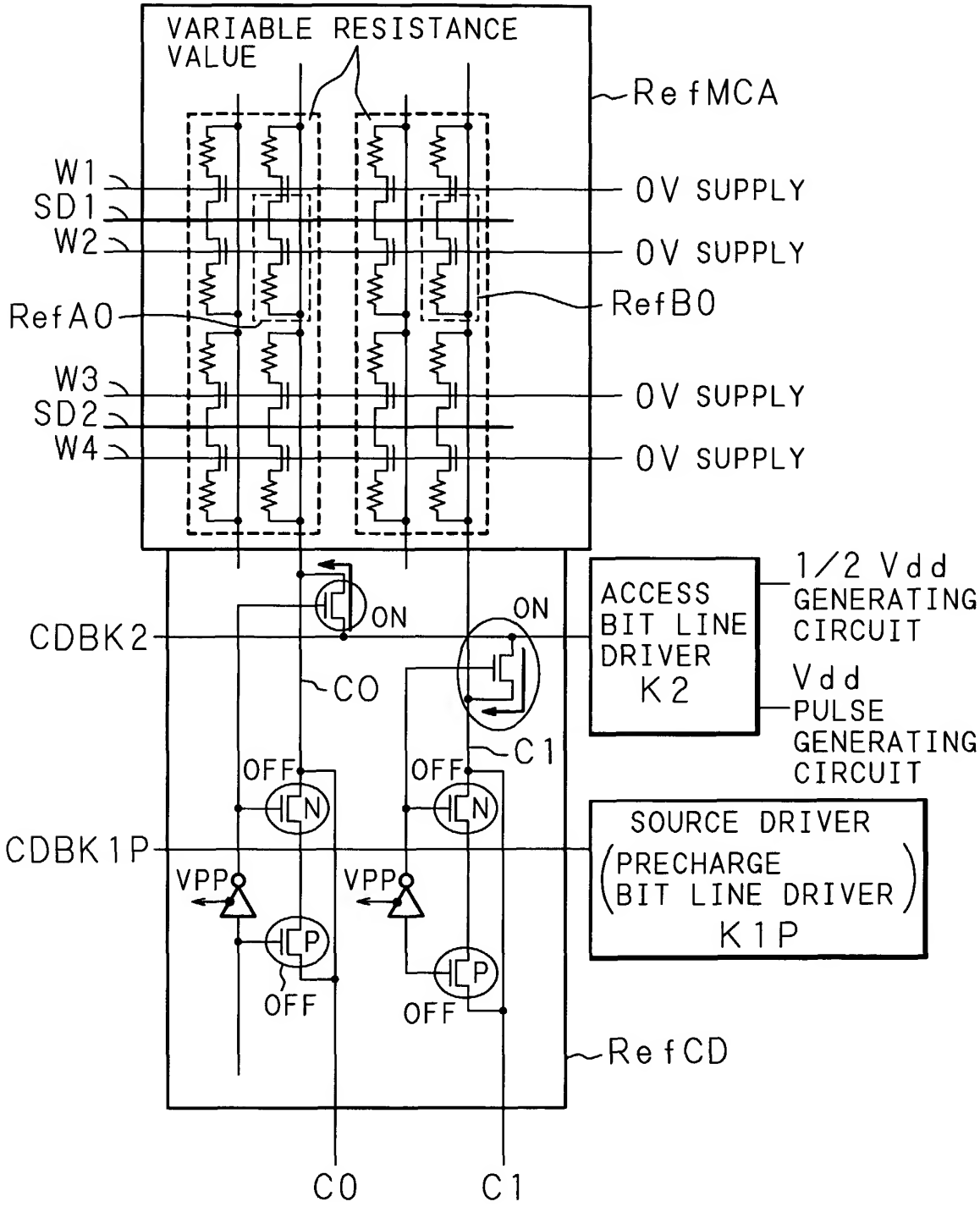

VARIABLE RESISTANCE VALUE
RefMCA
W1
SD1
W2
RefA0
W3
SD2
W4
0V SUPPLY
0V SUPPLY
RefB0
0V SUPPLY
0V SUPPLY
ON
ON
CDBK2
CO
C1
ACCESS BIT LINE DRIVER K2
1/2 Vdd GENERATING CIRCUIT
Vdd PULSE GENERATING CIRCUIT
OFF
OFF
N
N
CDBK1P
SOURCE DRIVER (PRECHARGE BIT LINE DRIVER) K1P
VPP
VPP
P
P
OFF
OFF
RefCD
C0
C1

FIG. 19

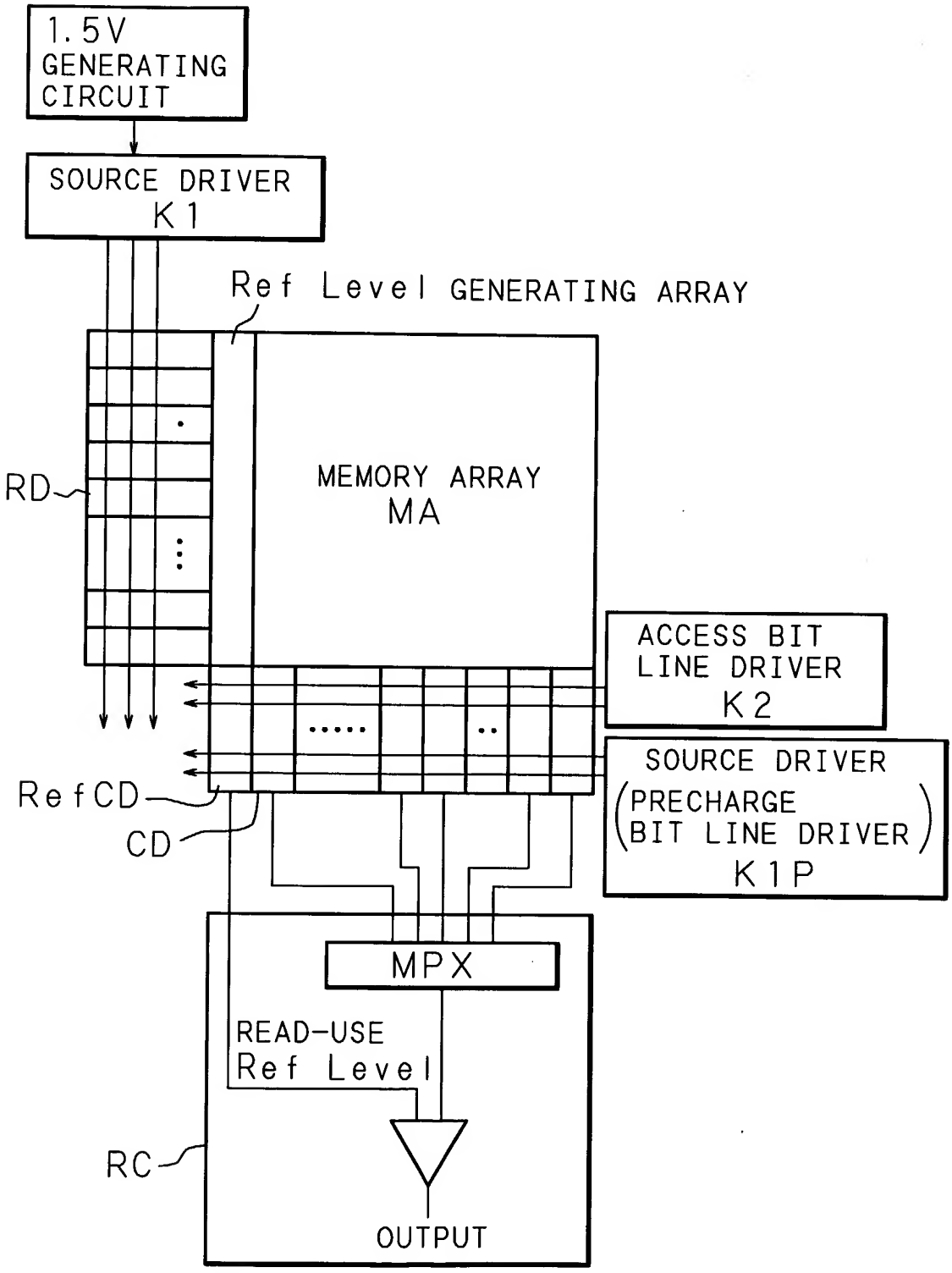

1.5V
GENERATING
CIRCUIT
SOURCE DRIVER
K1
Ref Level GENERATING ARRAY
RD
MEMORY ARRAY
MA
ACCESS BIT
LINE DRIVER
K2
SOURCE DRIVER
(PRECHARGE
BIT LINE DRIVER)
K1P
RefCD
CD
MPX
READ-USE
Ref Level
RC
OUTPUT

FIG. 20

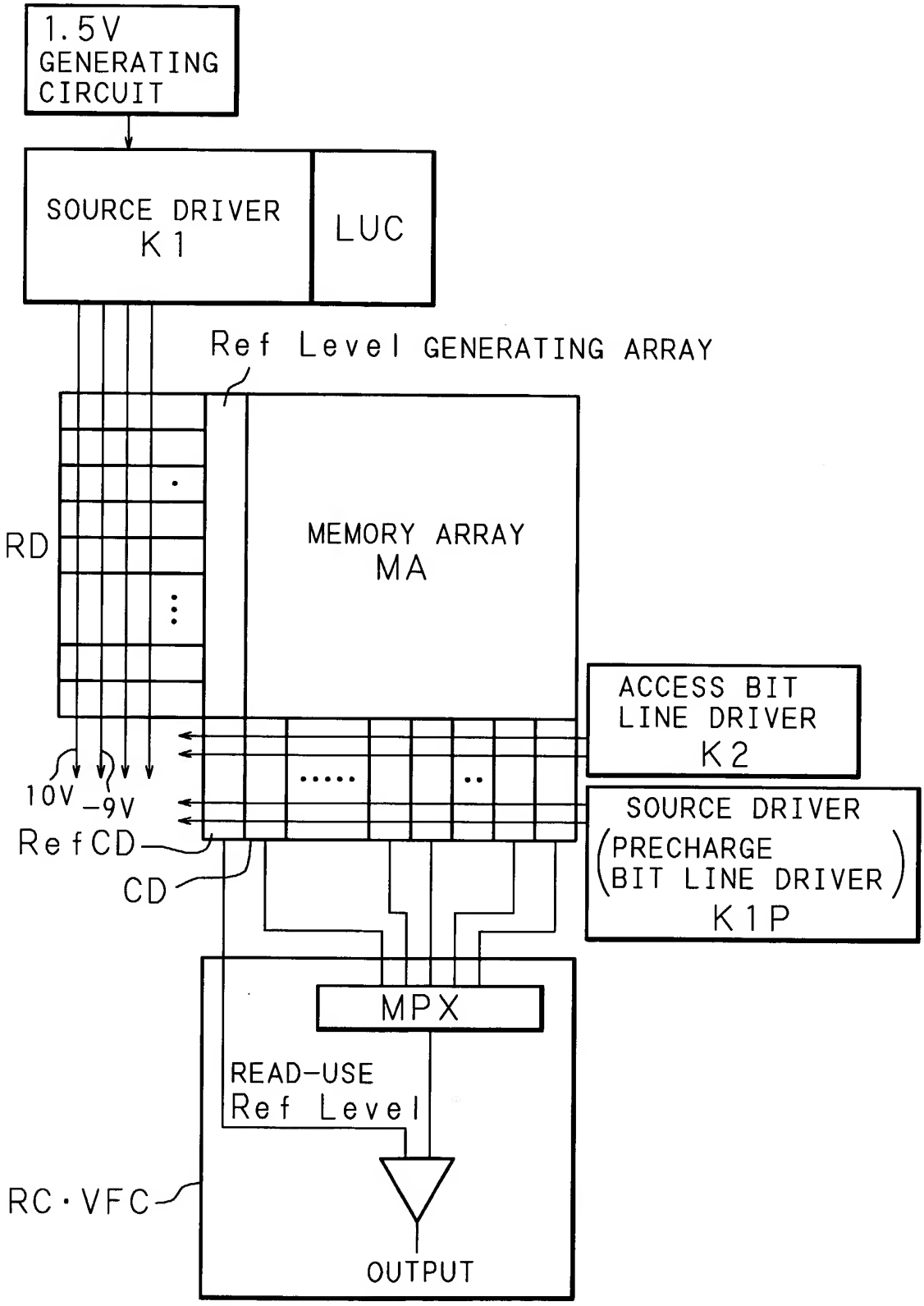

1.5V
GENERATING
CIRCUIT
SOURCE DRIVER
K1
LUC
Ref Level GENERATING ARRAY
RD
MEMORY ARRAY
MA
ACCESS BIT
LINE DRIVER
K2
10V
-9V
RefCD
CD
SOURCE DRIVER
(PRECHARGE
BIT LINE DRIVER)
K1P
MPX
READ-USE
Ref Level
RC·VFC
OUTPUT

FIG. 21A

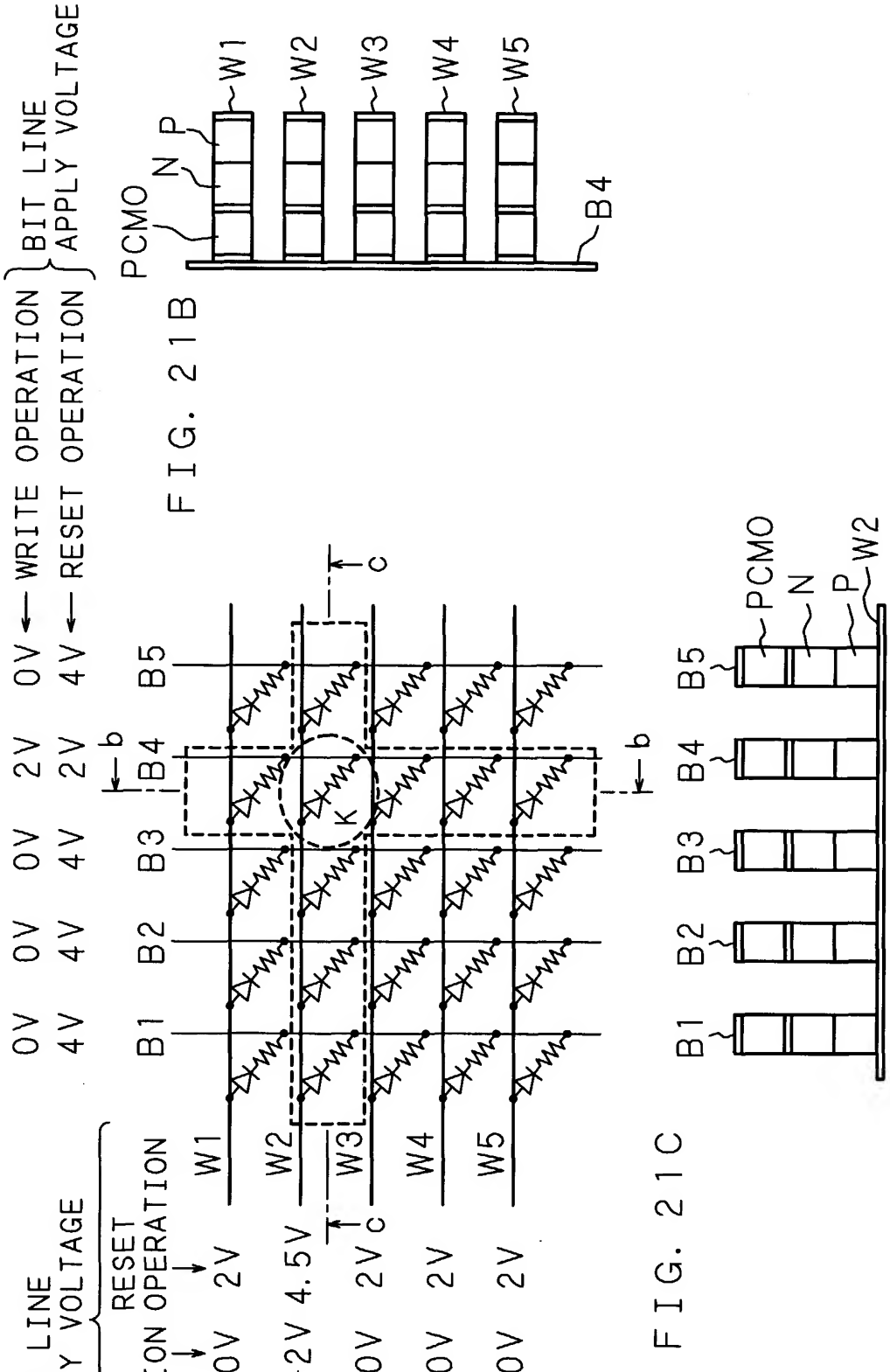


FIG. 21B

FIG. 21C

FIG. 22

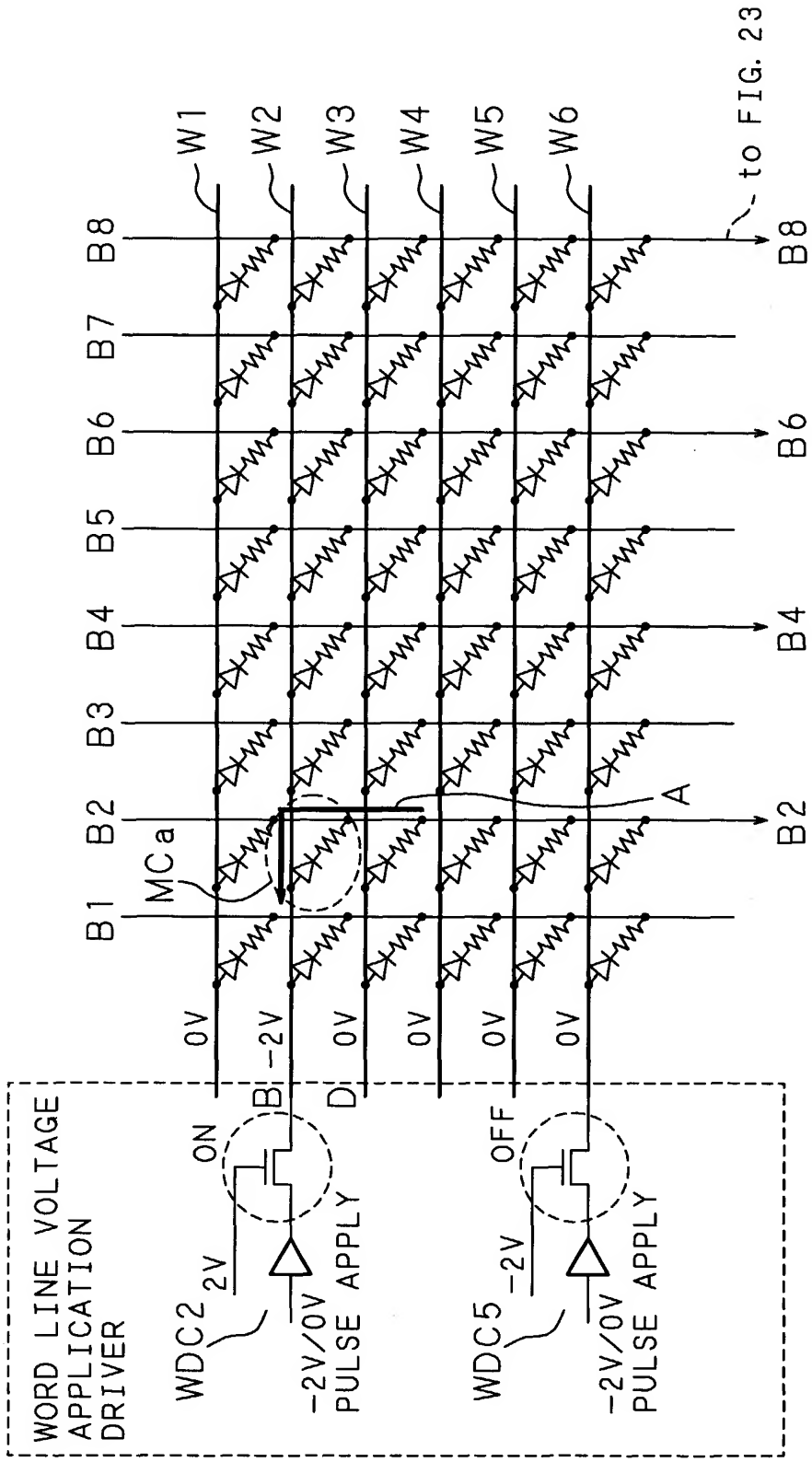

W1
W2
W3
W4
W5
W6
B8
B7
B6
B5
B4
B3
B2
B1
MCa
A
to FIG. 23
0V
-2V
0V
0V
0V
0V
B
D
ON
OFF
2V
-2V
WDC2
WDC5
-2V/0V
PULSE APPLY
-2V/0V
PULSE APPLY
WORD LINE VOLTAGE
APPLICATION
DRIVER

FIG. 23

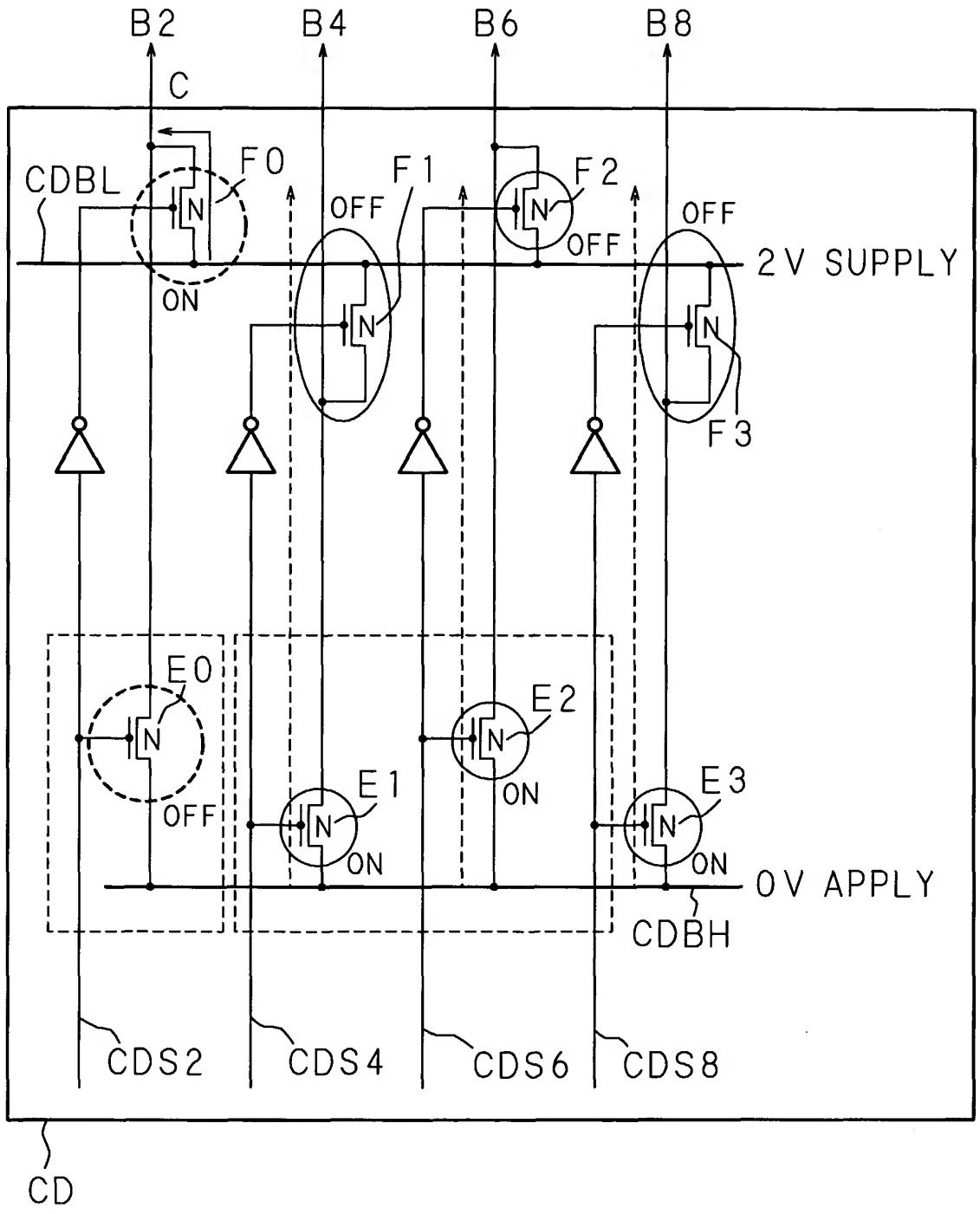

B2
B4
B6
B8
C
CDBL
F0
F1
F2
F3
N
OFF
ON
2V SUPPLY
E0
E1
E2
E3
0V APPLY
CDBH
CDS2
CDS4
CDS6
CDS8
CD

FIG. 24

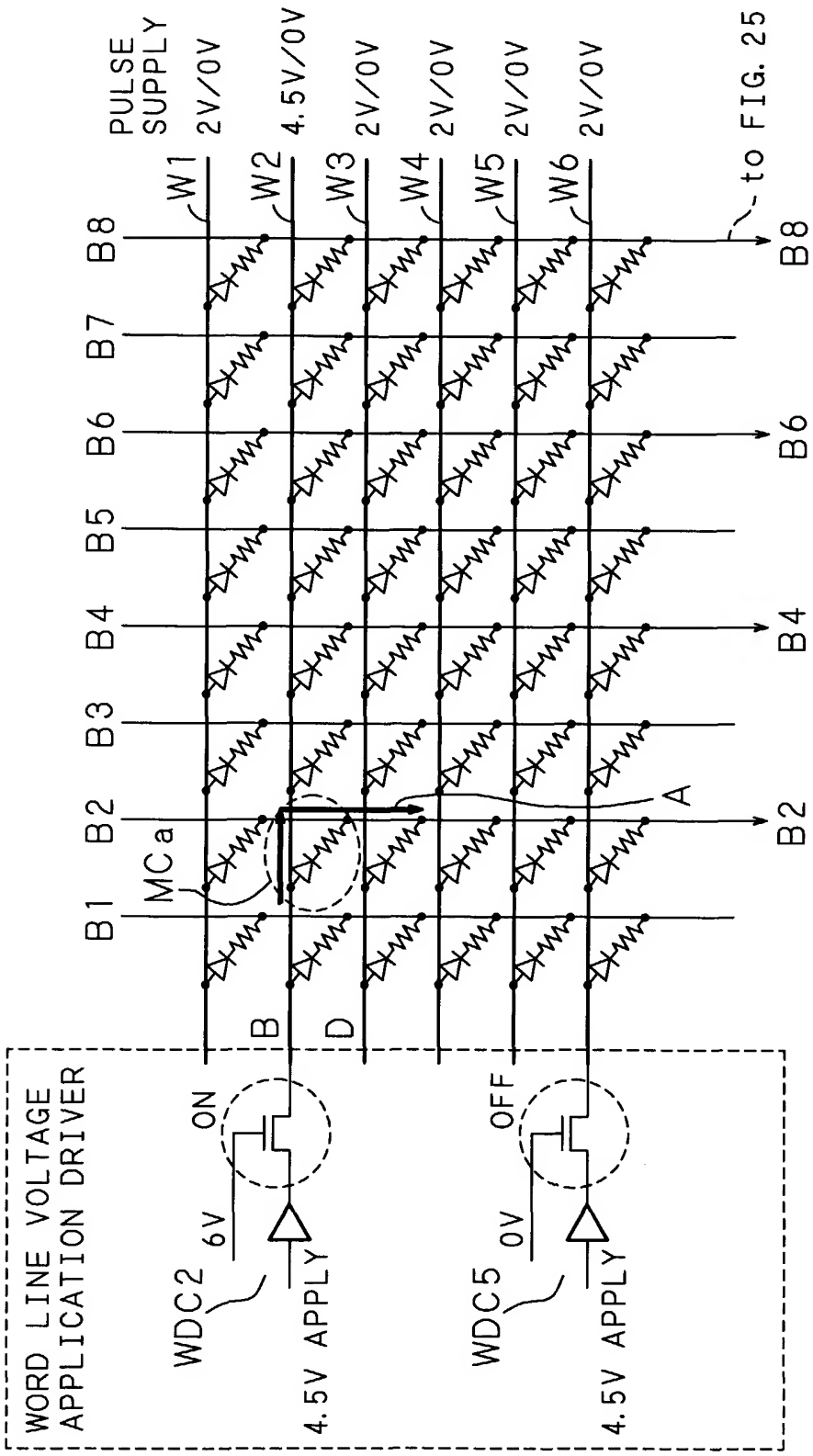
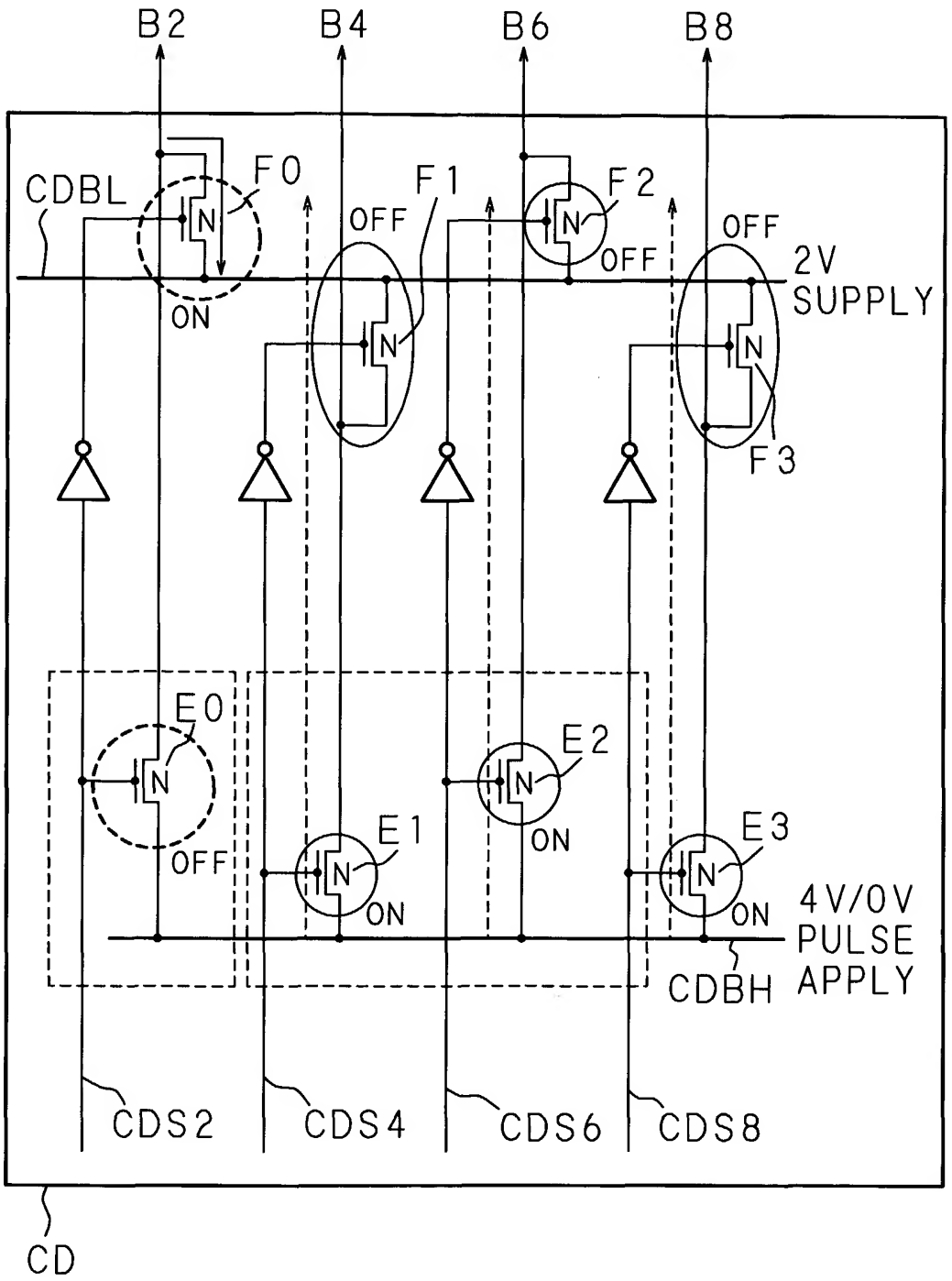

PULSE SUPPLY
2V/0V
4.5V/0V
2V/0V
2V/0V
2V/0V
2V/0V
W1
W2
W3
W4
W5
W6
to FIG. 25
B8
B7
B6
B5
B4
B3
B2
B1
MCa
A
B
D
WORD LINE VOLTAGE APPLICATION DRIVER
ON
OFF
6V
0V
WDC2
WDC5
4.5V APPLY
4.5V APPLY

FIG. 25


B2
B4
B6
B8
CDBL
F0
F1
F2
F3
N
OFF
ON
OFF
OFF
OFF
2V
SUPPLY
E0
E1
E2
E3
OFF
ON
ON
ON
4V/0V
PULSE
APPLY
CDBH
CDS2
CDS4
CDS6
CDS8
CD

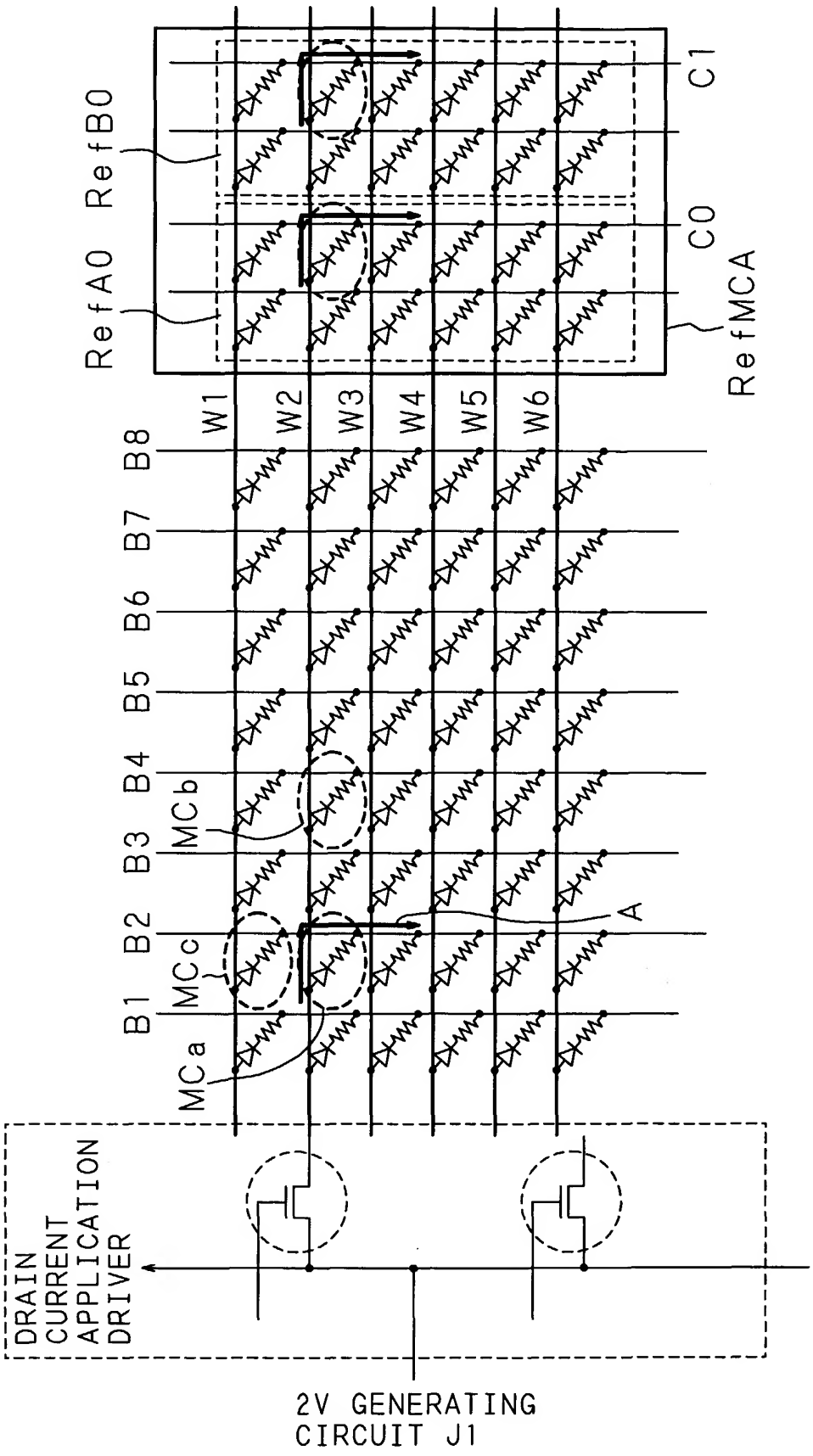

RefB0
RefA0
C1
C0
RefMCA
W1
W2
W3
W4
W5
W6
B8
B7
B6
B5
B4
B3
B2
B1
MCb
MCc
MCa
A
DRAIN CURRENT APPLICATION DRIVER
2V GENERATING CIRCUIT J1

FIG. 26

FIG. 27

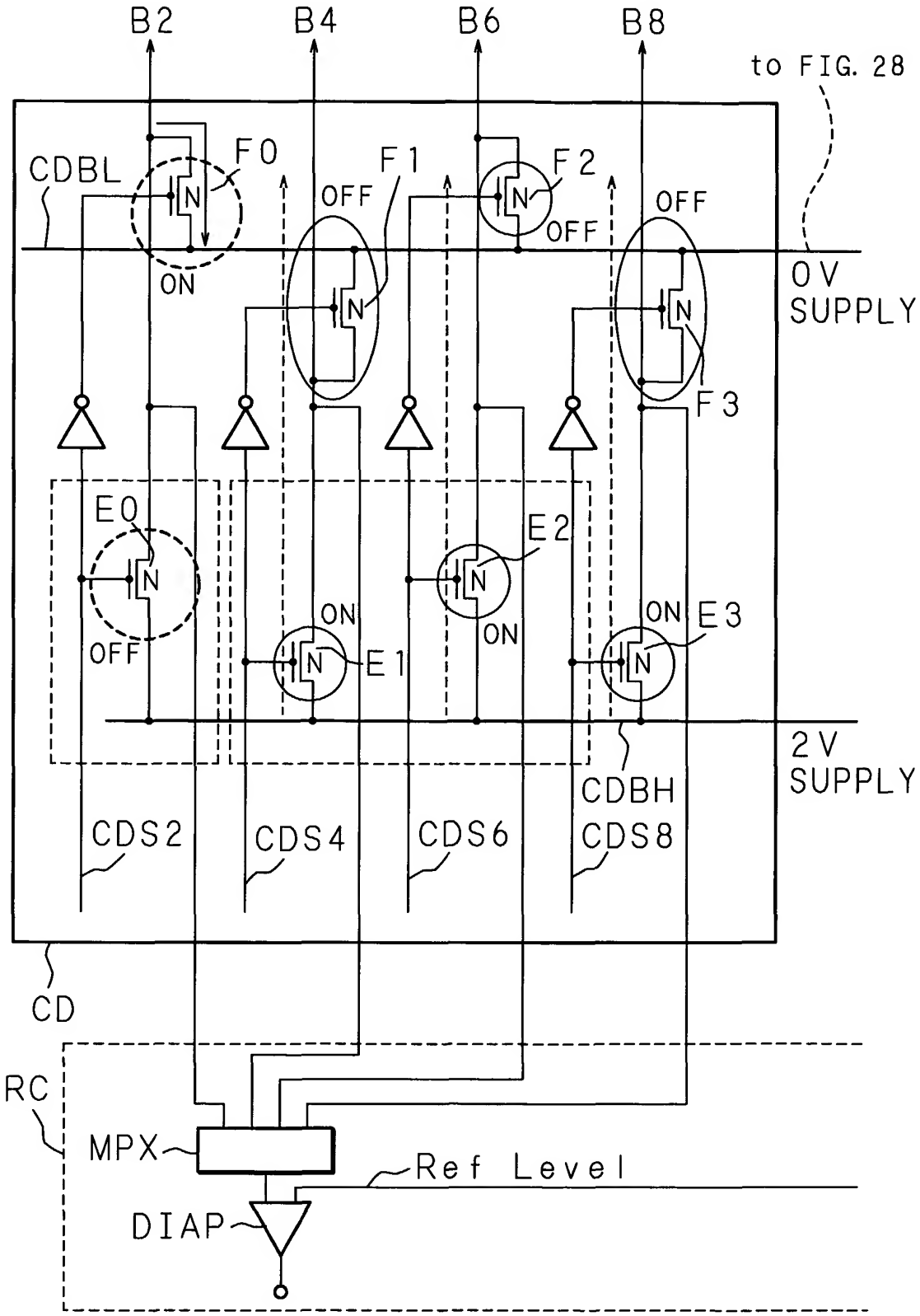

B2
B4
B6
B8
to FIG. 28
CDBL
F0
F1
F2
F3
OFF
ON
OFF
OFF
0V SUPPLY
E0
E1
E2
E3
ON
OFF
ON
ON
ON
2V SUPPLY
CDBH
CDS2
CDS4
CDS6
CDS8
CD
RC
MPX
Ref Level
DIAP

FIG. 28

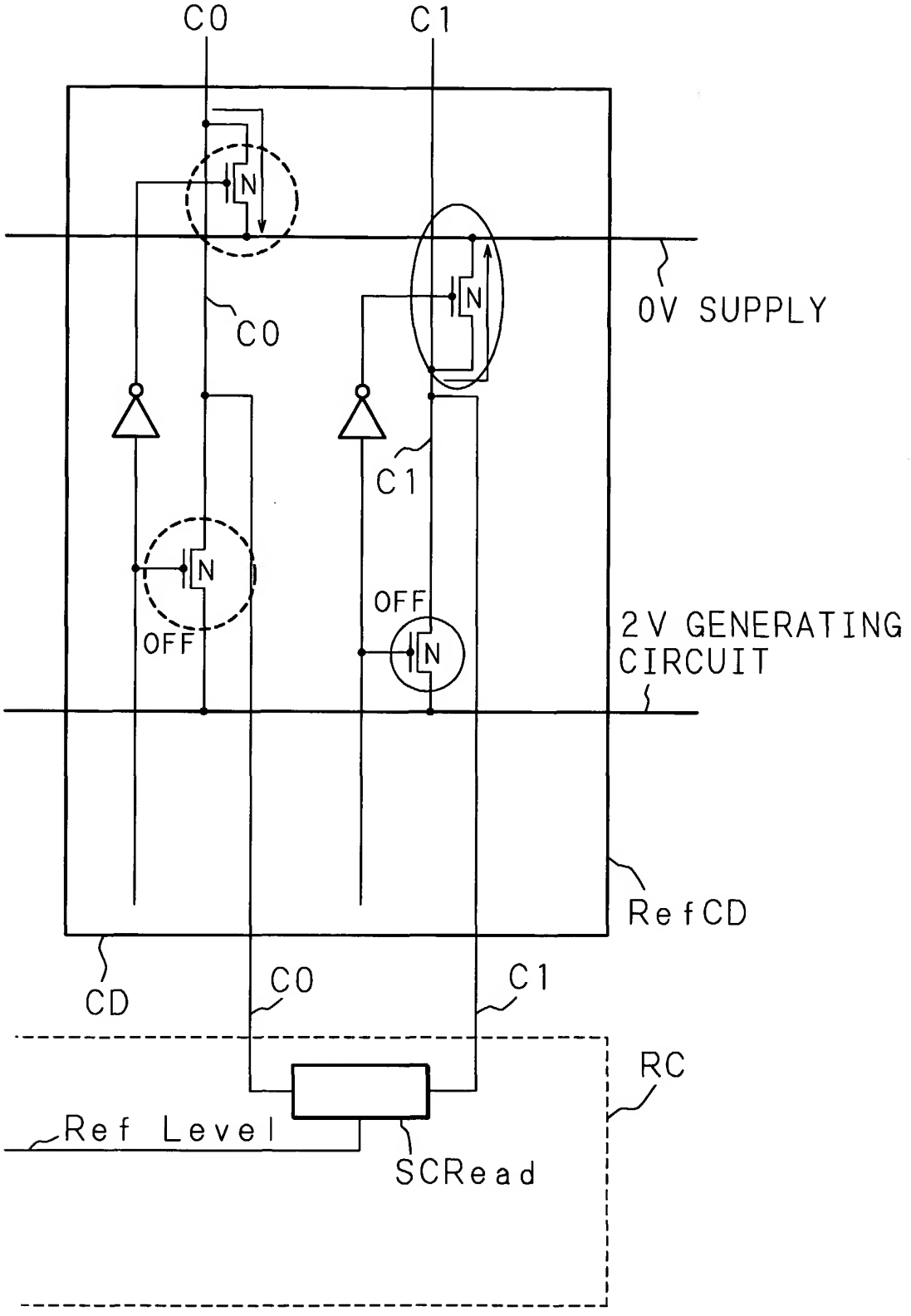

C0
C1
N
0V SUPPLY
C0
C1
OFF
2V GENERATING CIRCUIT
RefCD
CD
C0
C1
RC
Ref Level
SCRead

FIG. 29
PRIOR ART

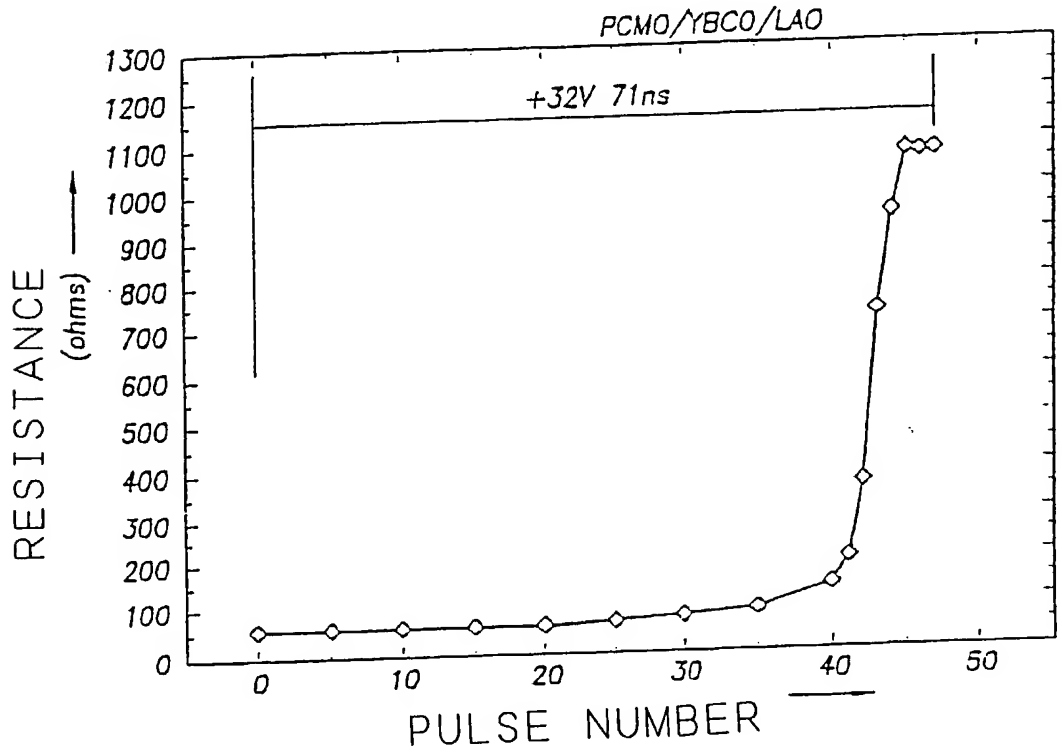


FIG. 30
PRIOR ART

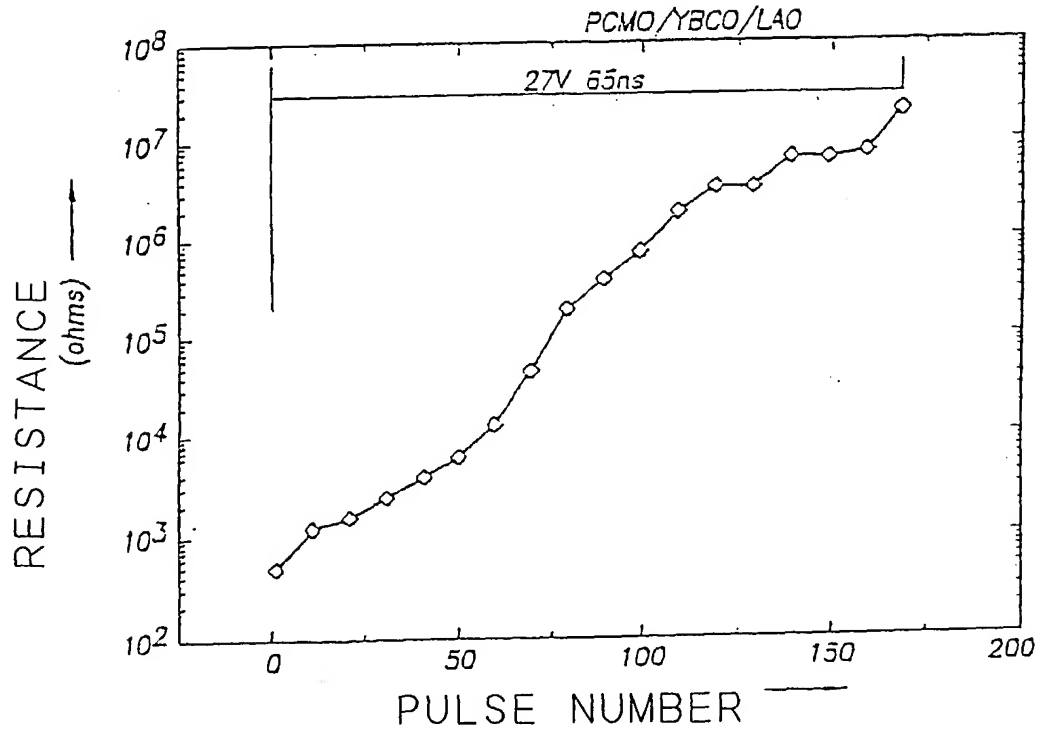


FIG. 31
PRIOR ART

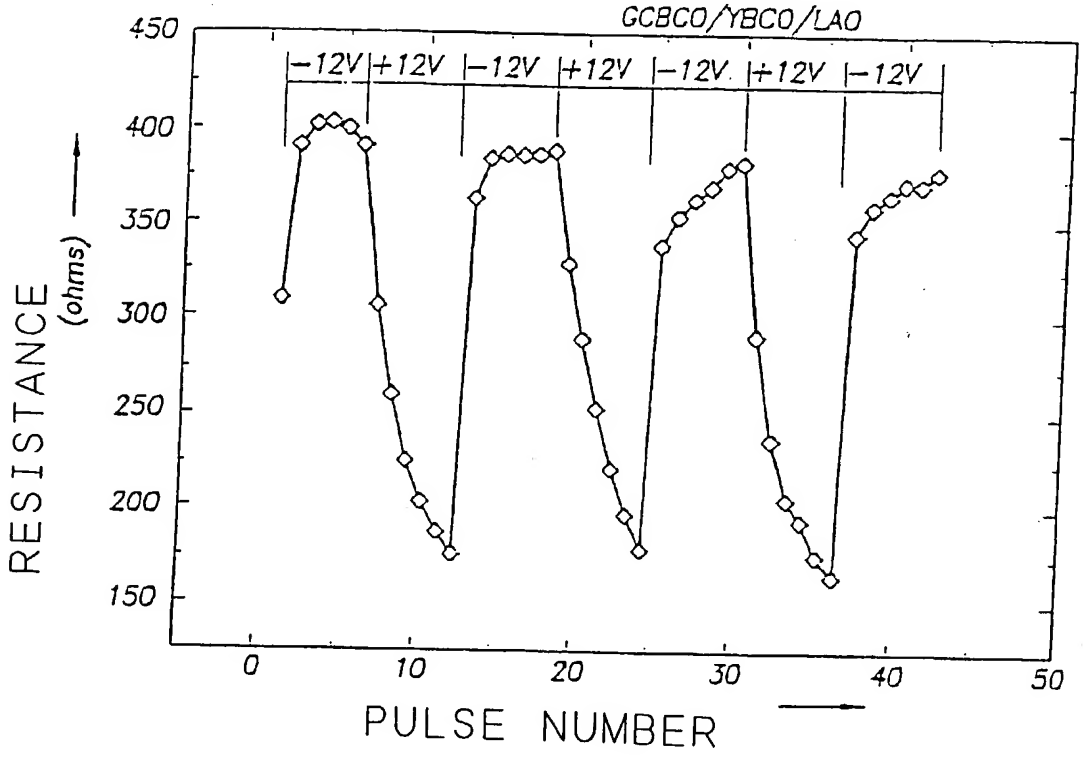


FIG. 32
PRIOR ART

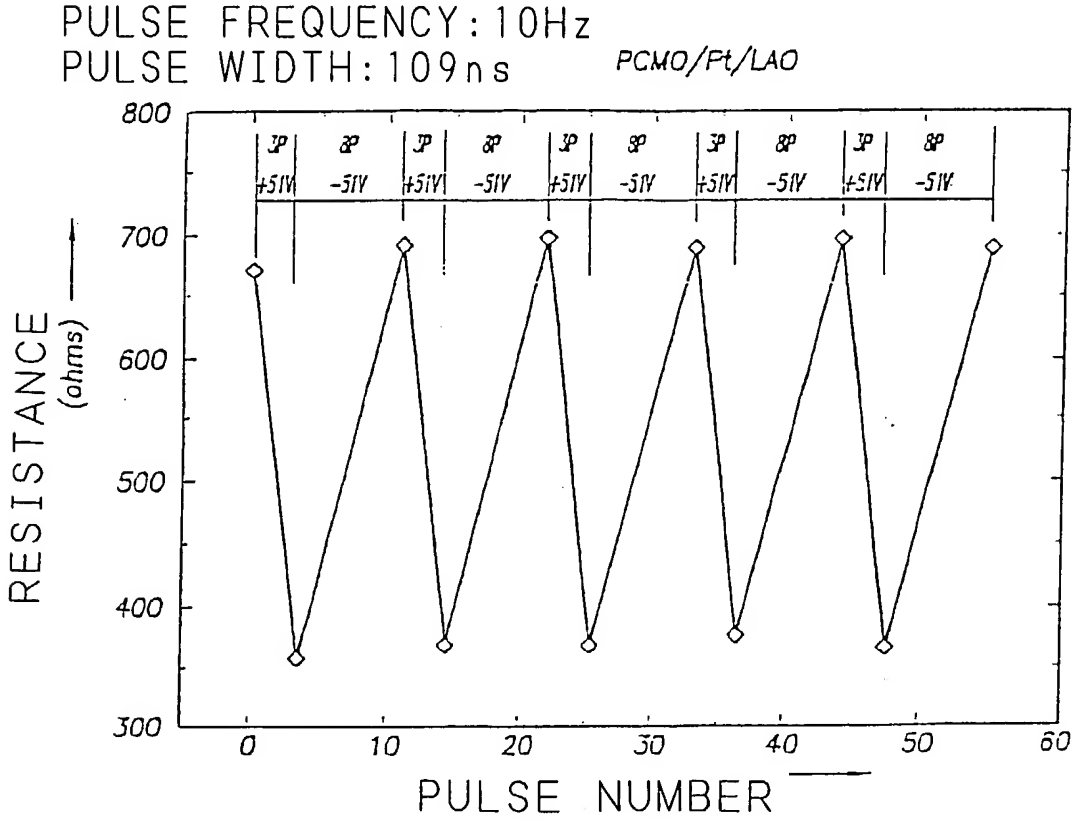
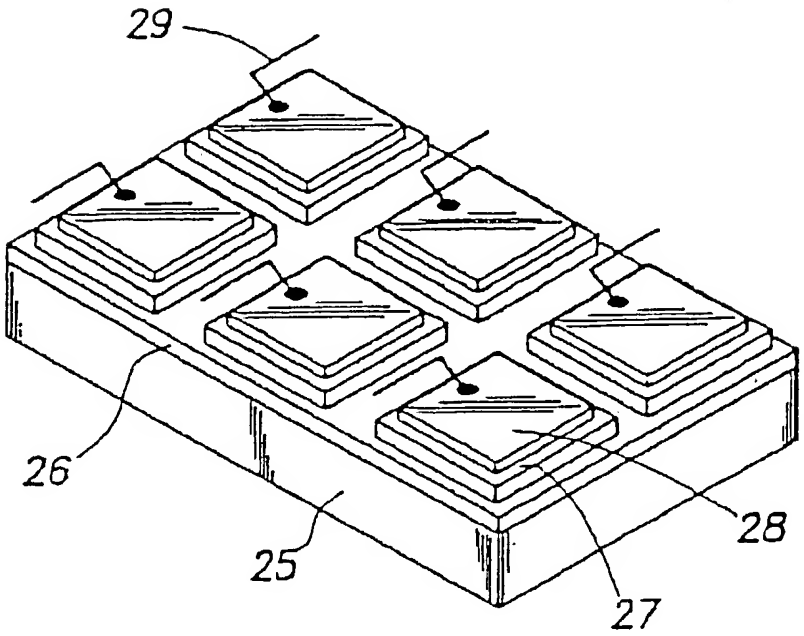


FIG. 33
PRIOR ART



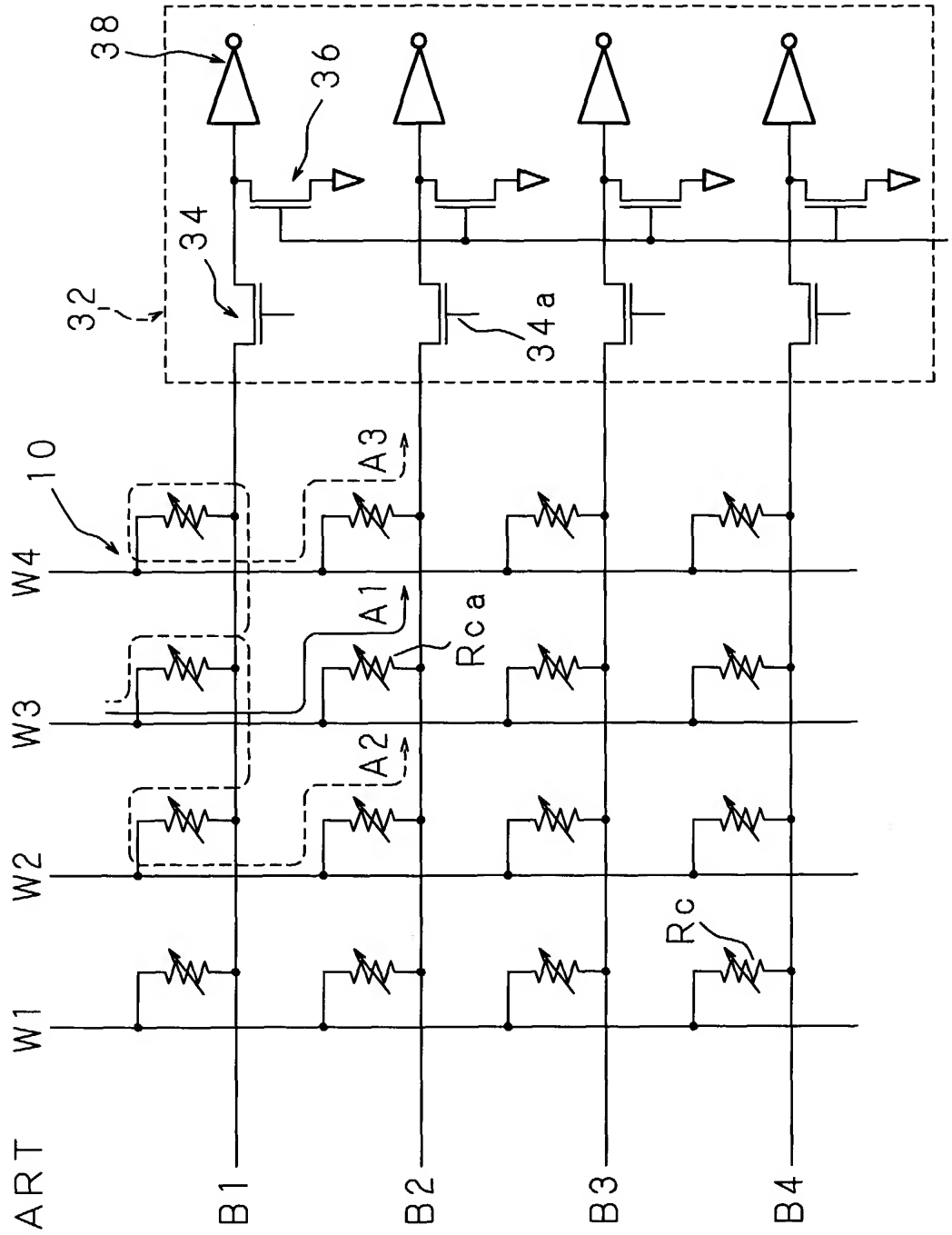


FIG. 34
PRIOR ART

FIG. 35

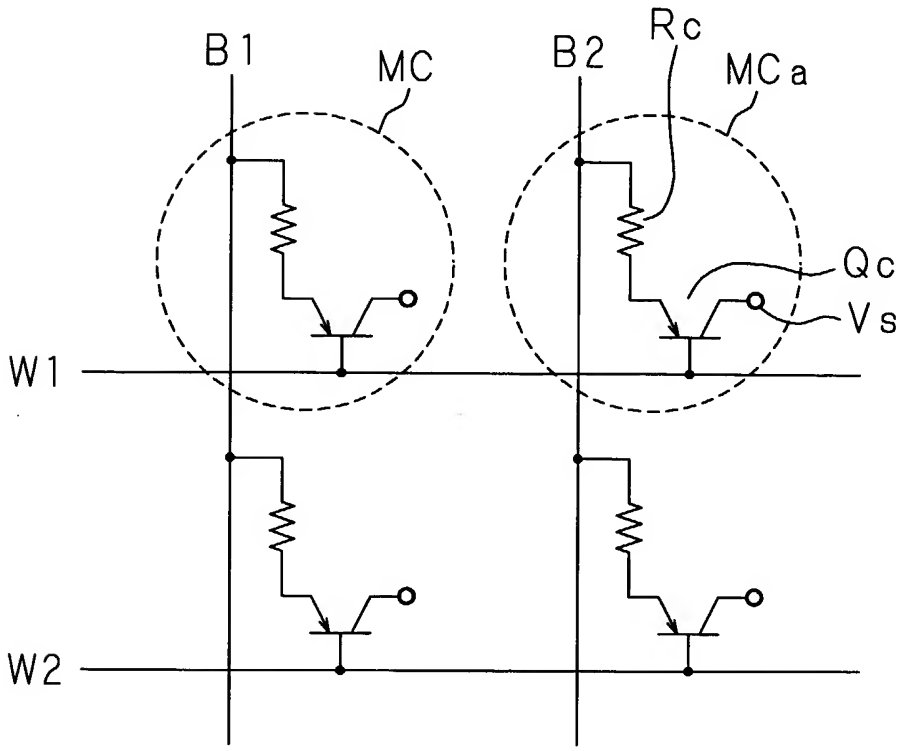


FIG. 36A

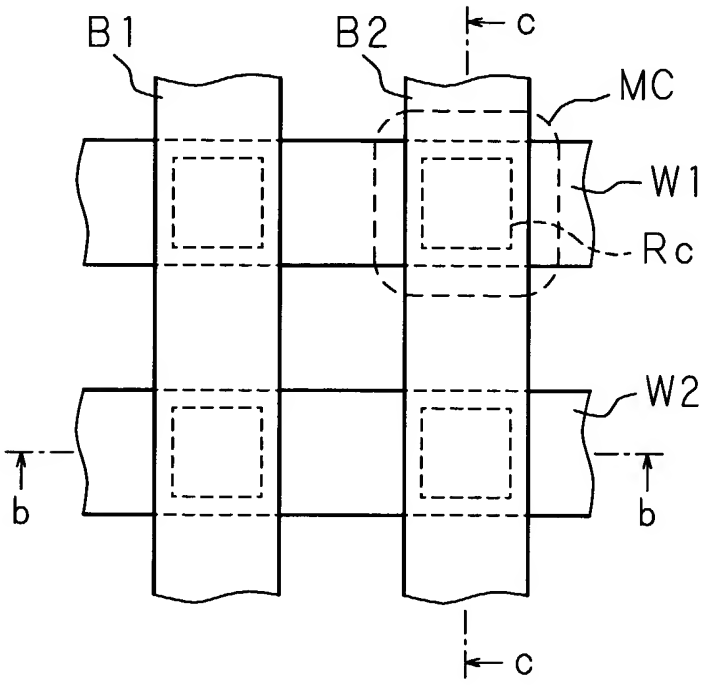


FIG. 36B

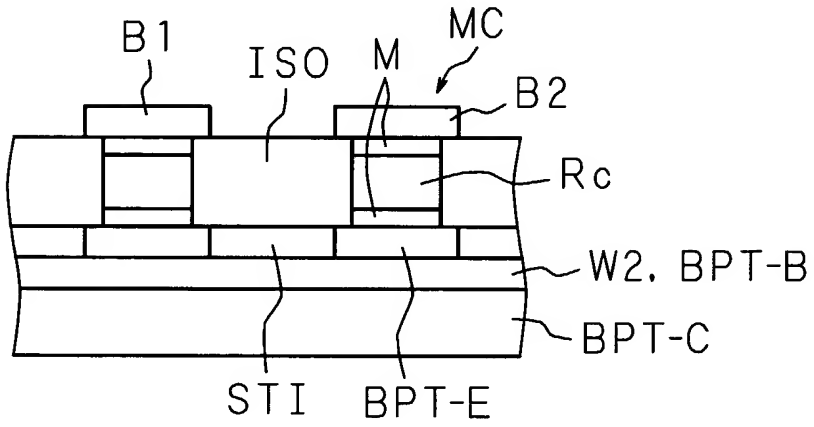


FIG. 36C